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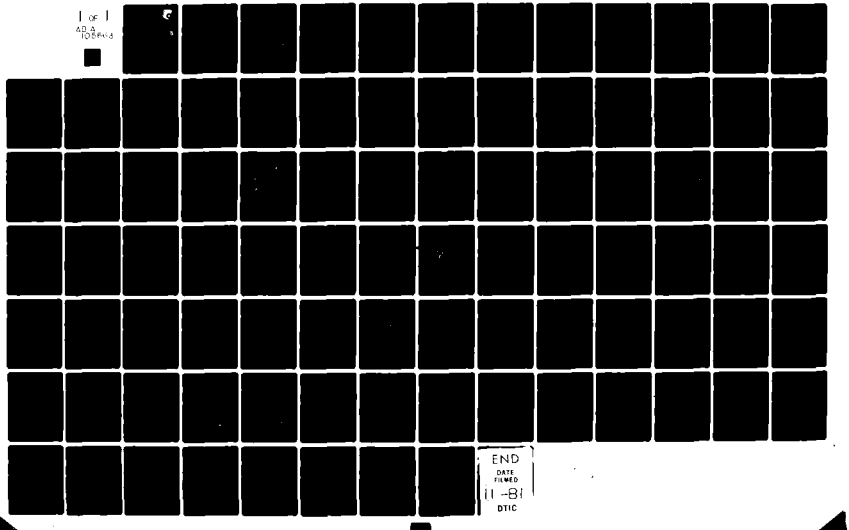

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DESIGN, PERFORMANCE AND DEVICE/CIRCUIT LIMITATIONS OF N-WAY SYMMETRICAL IMPATT DIODE POWER COMBINING ARRAYS

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August 1981

Interim Report for Period July 1979 to February 1981

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Circuit design and stability criteria are developed for a new class of IMPATT diode power combiners. These combiners make use of radial-symmetric circuits and provide an optimal integration of device and circuit properties to perform the power adding function. Both lossless N-way combiners and resistively stabilized N-way combiners are considered. Examples of this combining technique are given at frequencies of 10 GHz and 90 GHz which make use of realistic IMPATT diode parameters. The 30-W, ten-diode lossless X-band combiner indicates a 1-dB locking bandwidth of 300 MHz and 10 dB gain, while the millimeter-wave

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ABSTRACT (Cont)

combiner provides a 1-dB bandwidth of 9 GHz at 87 GHz and 10 dB locking gain. A 100-W, resistively stabilized 10 GHz, ten-diode combiner shows a 150 MHz locking bandwidth, also at 10 dB locking gain.

FOREWORD

This report describes the investigation of power combining studies at the Electron Physics Laboratory, Department of Electrical and Computer Engineering, The University of Michigan, Ann Arbor, Michigan. The work was sponsored by the Air Force Systems Command, Air Force Avionics Laboratory, Wright-Patterson Air Force Base, Ohio, under Contract No. F33615-77-C-1132.

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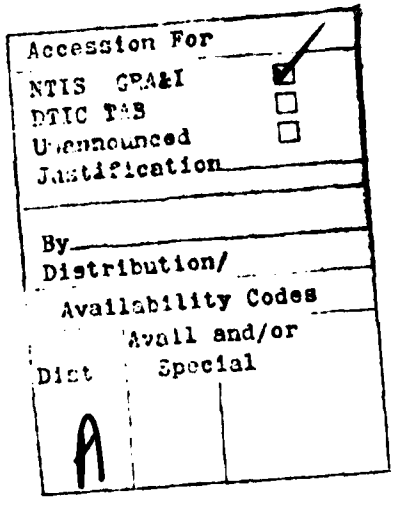

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1. Introduction

The purpose of this report is to present some new techniques and designs for circuit-level power combining of negative-resistance devices in general and IMPATT diodes in particular. In a recent review article, the present state of microwave power combining techniques was effectively summarized by Russell,[1] to which the reader is referred for an in-depth discussion of various combiner types and their performance. Basically, at the circuit level, combiners can be classified roughly into two categories, N-way, in which the outputs from all devices are combined in a single step, and corporate (hybrid) or serial, in which increasing power levels are successively combined. N-way combiners are often additionally separated into resonant and nonresonant structures. Examples of the former are the waveguide combiner of Kurokawa and Megalhaes[2] and the circular cylindrical TM_{ono} cavities of Harp et al.[3-6] Examples of the nonresonant N-way combiner include the nonplanar Wilkinson hybrid[7] and the five-way combiner of Rucker.[8]

Each of these power combining circuits has its associated performance limitations, design criteria, and problems. Corporate or serial combiners have the advantage of isolation between devices to eliminate deleterious interactions and provide broadband performance, but have the disadvantage of often substantial circuit and combining losses,[1] often at high power levels. Resonant N-way combiners require stabilization resistors to suppress device-device interactions and undesired oscillation modes in a high-Q cavity leading to narrow-band

although high-efficiency combining. Nonresonant N-way structures usually provide larger bandwidths with a corresponding increase in the mode suppression problem. Rucker's technique[8] analyzed by Kurokawa[9] has been successful, as has apparently been a conical line technique.[10] Radial arrays of equally spaced TEM lines have been used successfully for transistor power combining.[11]

The combining circuits analyzed in this report could perhaps be classified as N-way nonresonant transmission-line networks. As opposed to other networks of this type, however, the "circuit" and "device" properties are closely intertwined such that each cannot be specified independently. Hence the combiner represents, in some sense, an optimal integration of device and circuit to perform the power adding function. Both lossless and resistivity stabilized symmetrical combining circuits are considered and can provide the desired suppression of the unwanted, nonpower-producing modes while affording design flexibility in the power-producing mode. Lossless combiners require and make use of the band-limited negative-resistance properties of IMPATT diodes to provide stable and reasonably broadband operation. Values of TEM-line impedances, lengths, and stabilization resistances are determined by the IMPATT properties, rather than by conventional match and isolation requirements in power adders/dividers.[7,12] With negative-resistance diode terminations, the concept of "match" in particular is not, a priori, a useful condition.

Of particular importance in N-way combiners with active terminations is the suppression of all undesired modes of oscillation. For circuits with certain symmetry properties and identical active terminations, the various modes and their associated oscillation conditions

can be specified in all but unusual circumstances.[9] Circuit conditions for avoiding unwanted modes can then be investigated systematically. In Section 2, the basic combiner circuit and its symmetry properties are defined. The condition(s) for oscillation are reviewed and specified in terms of circuit eigenvectors and eigenvalues for the case of identical active devices. Appendix A expands on stability considerations and "other modes" of oscillation arising from nonlinear and nonidentical active device terminations.

Radially symmetric lossless TEM-line combiners having N-1 eigenvalue degeneracy are analyzed with examples in Section 3. It is shown that diode properties specify combiner TEM-line characteristic impedance and line length for unwanted mode suppression and that circuit design for the power-producing mode is relatively straightforward. Examples are given for a 30-W, ten-diode, X-band microstrip combiner and a millimeter-wave (90 GHz) combiner. The effect of diode failure in those lossless circuits (Appendix B) is seen to be fairly "graceful" by usual standards.

Resistive-stabilized TEM-line symmetric combiners are discussed in Section 4. Examples of practical and realizable stabilization networks and their relation to diode and combiner properties are given. Values of stabilizing resistors are specified in terms of device negative conductance level and the number of diodes combined. As an example, a detailed analysis of a 100-W, ten-diode, X-band microstrip combiner is presented.

An overall summary of the results, conclusions and comparison with other techniques is given in Section 5.

2. Combiner Description and Stability Considerations

Combiner Description. A general power combining network for use with negative-resistance devices is shown in Fig. 1. The combiner has N ports for active device terminations and one port for common excitation and output power extraction. It is assumed that the combiner has certain symmetry properties such that its admittance matrix $\underline{Y}_c$ can be written as

$$\underline{Y}_c = \begin{bmatrix} y_{oo} & y_{od} & y_{od} & \cdots & y_{od} \\ y_{od} & & & & \\ y_{od} & & \underline{Y} & & \\ \vdots & & & & \\ y_{od} & & & & \end{bmatrix} , \qquad (1)$$

where the N x N matrix $\underline{Y}$ defined as

$$\underline{Y} \triangleq [y_{mn}] \qquad (2)$$

has the element properties that

$$y_{m+k,n+k} = y_{mn} = y_{nm} , \qquad (3)$$

where the subscripts are modulo N. The interpretation of Eq. 3 is that the combiner has radial symmetry with any row of $\underline{Y}$ a "rolled" version of any other row. Along with reciprocity, this implies that $\underline{Y}$ has at most N/2 + 1 distinct elements if N is even and (N + 1)/2 distinct elements if N is odd. Except for certain hybrid, resonant cavity[2] and graduated coupling structures, most useful power combiners have the symmetry properties indicated above.

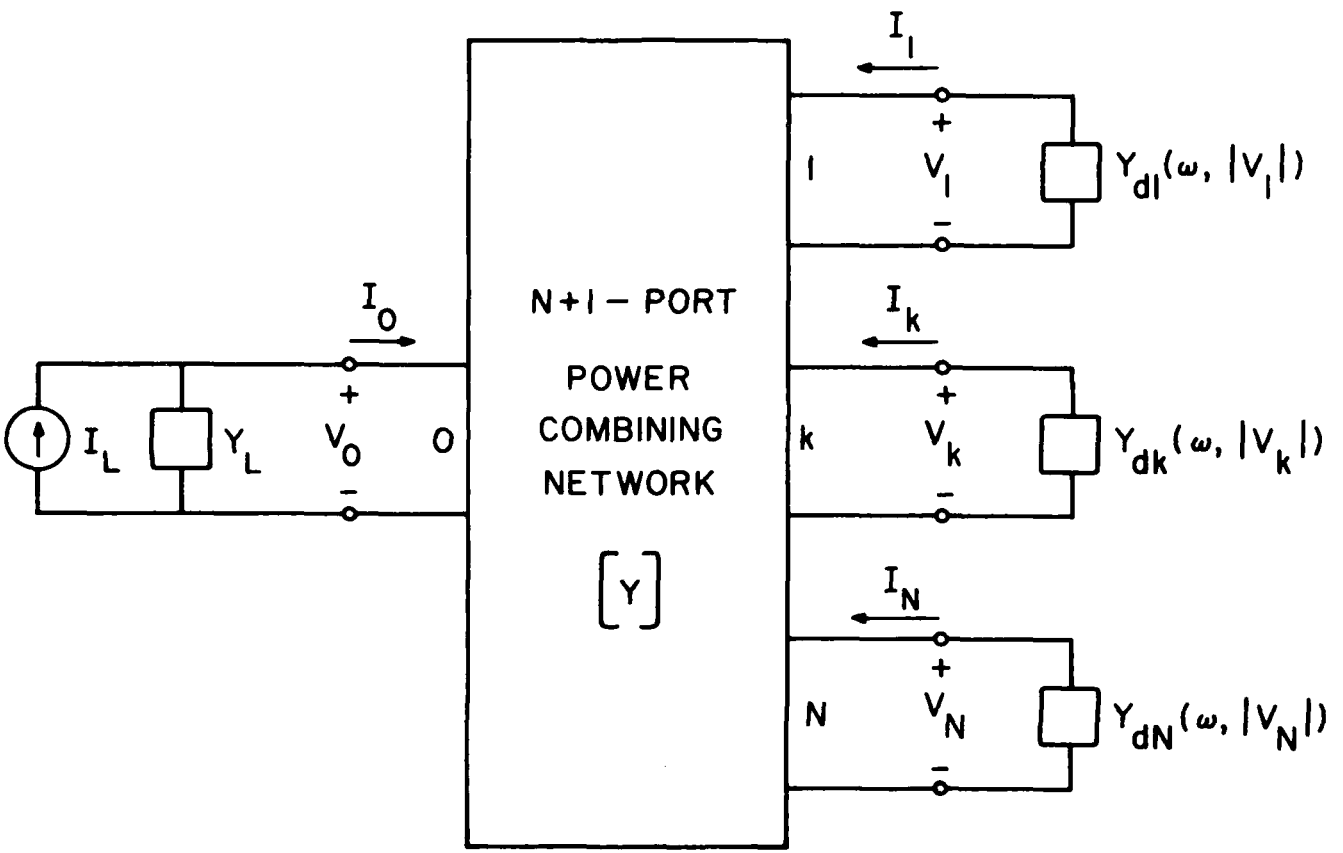


FIG. 1 A GENERAL, N-NEGATIVE-RESISTANCE-DIODE POWER-COMBINING NETWORK.

Terminations. Ports 1 through N of the combiner will be terminated in active, nonlinear devices. It is assumed that the device on port k, $1 \leq k \leq N$ can be represented by its admittance describing function $Y_{dk}(\omega,|V_k|)$, where $|V_k|$ is the amplitude of the RF voltage at port k and ω is the frequency. At port 0, the termination is $Y_L(\omega)$ with excitation I_L. The termination matrix $\underline{Y}_t$ is thus written as

$$\underline{Y}_t = \text{diag}[Y_L(\omega), Y_{d1}(\omega,|V_1|),\ldots,Y_{dN}(\omega,|V_N|)] \quad . \tag{4}$$

Condition for Oscillation. Of particular interest for multidiode combiners is system stability when devices are capable of interacting with one another. The condition for oscillation for the combiner can be written as

$$(\underline{Y}_c + \underline{Y}_t)\underline{V} = \underline{0} \quad , \tag{5}$$

where

$$\underline{V} = [V_o \; V_1 \; V_2 \; \ldots \; V_N]^+ \tag{6}$$

is the vector of port voltages and $\underline{0}$ is the empty vector. For a given termination Y_L at port 0,

$$V_o = - \frac{y_{od} \sum_{k=1}^{N} V_k}{y_{oo} + Y_L} \tag{7}$$

and the condition for oscillation becomes

$$(\underline{Y}' + \underline{Y}'_t)\underline{V}' = \underline{0}' \quad , \tag{8}$$

where the primed quantities are associated only with ports 1 to N, and the elements of $Y' = [y'_{mn}]$ are given by

$$y'_{mn} = y_{mn} - \frac{y_{od}^2}{y_{oo} + Y_L} \quad . \tag{9}$$

The matrix $\underline{Y}'$ retains the symmetry properties of $\underline{Y}$. Nontrivial solutions to Eq. 8 are the modes of oscillation for the system.

Modes of Oscillation. The eigenvectors $\underline{x}_k$ and associated eigenvalues λ_K for the symmetric matrix $\underline{Y}'$ are obtained from

$$\underline{Y}'\underline{x}_k = \lambda_k \underline{x}_k \tag{10}$$

and are given by

$$\underline{x}_k = \frac{1}{\sqrt{N}} \begin{bmatrix} 1 \\ e^{jka} \\ e^{j2ka} \\ \vdots \\ e^{j(N-1)ka} \end{bmatrix} \quad , \quad k = 0 \text{ to } N-1 \tag{11}$$

and

$$\lambda_k = \sum_{n=1}^{N} y'_{mn} e^{jka(n-1)} \quad , \quad k = 0 \text{ to } N-1 \quad , \quad \text{any } m \tag{12}$$

where $a = 2\pi/N$. The eigenvector $\underline{x}_o$ and corresponding eigenvalue λ_o are associated with the in-phase desired power-producing mode for the combiner, while the other $\underline{x}_k$ and λ_k are associated with "rotating" or anti-phase modes of no output. Using Eq. 9 in Eq. 12 shows that

$$\lambda_o = \sum_{n=1}^{N} y_{mn} - \frac{N y_{od}^2}{Y_{oo} + Y_L} \quad , \quad \text{any } m \tag{13a}$$

and

$$\lambda_k = \sum_{n=1}^{N} y_{mn} e^{jka(n-1)} \quad , \quad \text{any } m \quad , \quad k = 1 \text{ to } N-1 \quad . \tag{13b}$$

Hence, the λ_k, $1 \leq k \leq N-1$ are the same for the matrices $\underline{Y}$ and $\underline{Y}'$ and are independent of the load admittance. The number of distinct eigenvalues is the same as the number of distinct values of the y_{mn}, which is $N/2 + 1$ for N even and $(N+1)/2$ if N is odd.

Possible solutions to Eq. 8 are now seen to be

$$-\underline{Y}'_t = \lambda_k \underline{I} \quad \text{for } \underline{V}' = \sqrt{N}\, V \underline{x}_k \quad , \tag{14}$$

where $V = |V_n|$, $1 \leq n \leq N$, or equivalently

$$-Y_{dn}(j\omega, |V_n|) = -Y_d(j\omega, V) = \lambda_k(j\omega) \quad , \tag{15}$$

i.e., all Y_{dn} are the same. In this case, the zeroth mode (λ_o) is the power-producing mode and would require a stable solution to

$$-Y_d(j\omega, V) = \lambda_o(j\omega) \tag{16}$$

for oscillation. Any stable antiphase modes characterized by $\Sigma V_k = 0$ ($V_o = 0$ from Eq. 7) would need to be suppressed for the combiner to operate properly. In this case of identical active devices, circuit design must provide the proper value of λ_o for oscillation or amplification while suppressing the other modes. Since the λ_k in Eq. 13b are independent of Y_L and depend only on the inherent properties of the combiner circuit, a stable, even-mode-only design is possible in principle.

Other Modes. Additional modes to those outlined above are possible in the combiner because the devices are nonlinear and can be nonidentical. One such mode, pointed out by Kurokawa,[9] was based on a perturbation analysis and found to be very unlikely to exist because of the device-circuit relation required. The case of other modes is treated in Appendix A, where more general stability conditions than Kurokawa's are derived. The results seem to indicate that other modes require that unusual device-circuit conditions exist, at least when the devices are nearly identical.

3. Lossless, Radial-Symmetric, TEM-Line Combiners

Degenerate Eigenvalue Networks. A combining network which is lossless and obeys the symmetry properties given in Section 2 has eigenvalues λ_k, $1 \leq k \leq N$, that are purely imaginary since the y_{mn} in Eq. 13b are all imaginary. Clearly, for the rotating modes, all the power into the network must be returned. Hence, rotating mode suppression under active device terminations in such a combiner requires that there are some lossless networks which can terminate the active device in a stable manner and that these networks are realizable in a power combining circuit and represent the λ_k's.

These criteria can be achieved using IMPATT diodes and a simple TEM-line power combining circuit. Under certain conditions, the band-limited negative-resistance properties of IMPATT diodes in combination with TEM lines of suitable length and characteristic impedance can provide a stable combiner in which only the even mode can exist.

The simplest combiner of this type is a TEM-line network as shown in Fig. 2. An array of identical transmission lines is placed

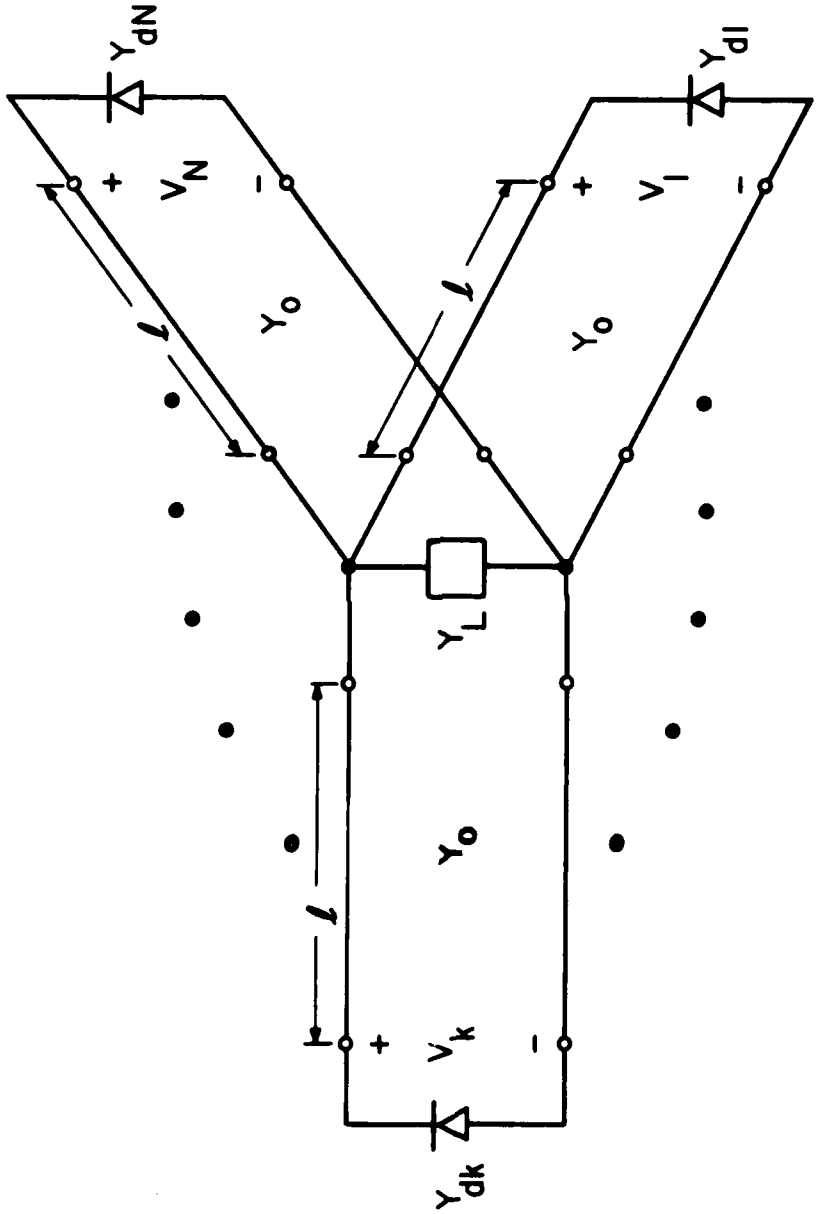


FIG. 2 A TEM-LINE COMBINING NETWORK PROVIDING N - 1 DEGENERATE EIGENVALUES FOR THE ROTATING MODES.

symmetrically around a "hub" where power is extracted, with the lines terminated in IMPATT diodes. For this network, it is assumed that

$$y_{mn} = 0 \quad , m \neq n \tag{17}$$

so that the eigenvalues λ_k are degenerate and

$$\lambda_k = y_{11}(j\omega) = - jY_o \cot \beta\ell \quad , \quad 1 \leq k \leq N \tag{18}$$

for all the rotating modes. The eigenvalue λ_o associated with the even mode is then given by

$$\lambda_o = - jY_o \cot \beta\ell + \frac{NY_o^2 \csc^2 \beta\ell}{Y_L - jY_o \cot \beta\ell} \quad , \tag{19}$$

where β is the propagation factor, so that λ_o represents the input admittance of a TEM line terminated in an effective admittance of Y_L/N.

The assumption of eigenvalue degeneracy, or equivalently, zero coupling between lines simplifies the design problem and illustrates the appropriate device-circuit interaction for stability. This criteria can be approximately met in practice, especially if the number of diodes is not too large. For slight coupling between lines, such that the eigenvalues are not too different, an appropriate design can still be achieved in many cases. This point will be clarified later in this section.

Rotating Mode Stability. Stability of the rotating modes for the degenerate case requires that there be no stable solutions to

$$Y_d(j\omega,V) - jY_o \cot \beta\ell = 0 \quad , \tag{20}$$

for any combination of ω and V, where identical diodes have been assumed, or equivalently,

$$\mathrm{Re}\{Y_d(j\omega,V)\} \triangleq G_d(\omega,V) = 0 \qquad (21a)$$

and

$$\mathrm{Im}\{Y_d(j\omega,V)\} \triangleq B_d(\omega,V) = Y_o \cot \beta\ell \ . \qquad (21b)$$

If $V_o(\omega)$ is the voltage required at any ω to satisfy Eq. 21a, then the associated diode susceptance $B_{dg}(\omega)$ is obtained as

$$B_{dg}(\omega) = B_d[\omega,V_o(\omega)] \ . \qquad (22)$$

Since the IMPATT diode has a band-limited negative conductance, any solutions to Eqs. 20 or 21 need be considered only over a certain band of frequencies. A typical plot of the nonlinear admittance properties of an IMPATT diode is shown in Fig. 3, indicating the limited negative-resistance bandwidth. The conductance first becomes negative near the "avalanche" frequency, goes through a maximum and becomes positive again at a frequency determined by the device carrier transit time. Of importance in Eqs. 20 or 21 is that large-signal levels can decrease the diode conductance, especially at the lower frequencies. In fact, a passive admittance at small signal levels can become active for certain drive levels and frequencies. As evident, the effect of this is to make the solution to Eq. 21a double valued, providing two values of B_{dg} at some frequencies. This must be considered when designing to avoid the conditions of Eqs. 20 or 21.

Several types of device and circuit interactions are indicated in Fig. 4, where $B_{dg}(\omega)$ is compared to several circuit functions

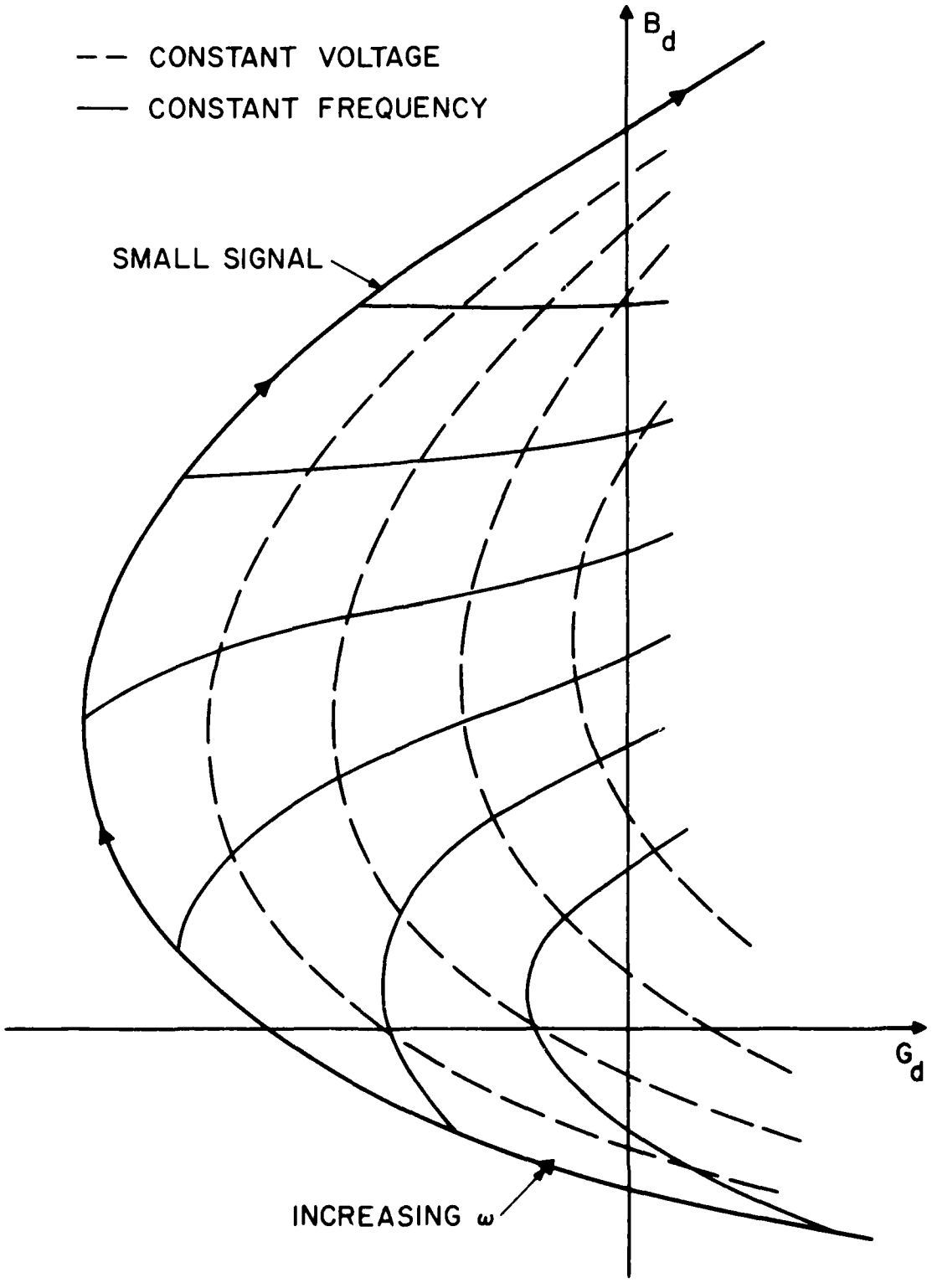


FIG. 3 A TYPICAL ADMITTANCE PLANE PLOT OF THE NONLINEAR PROPERTIES OF AN IMPATT DIODE.

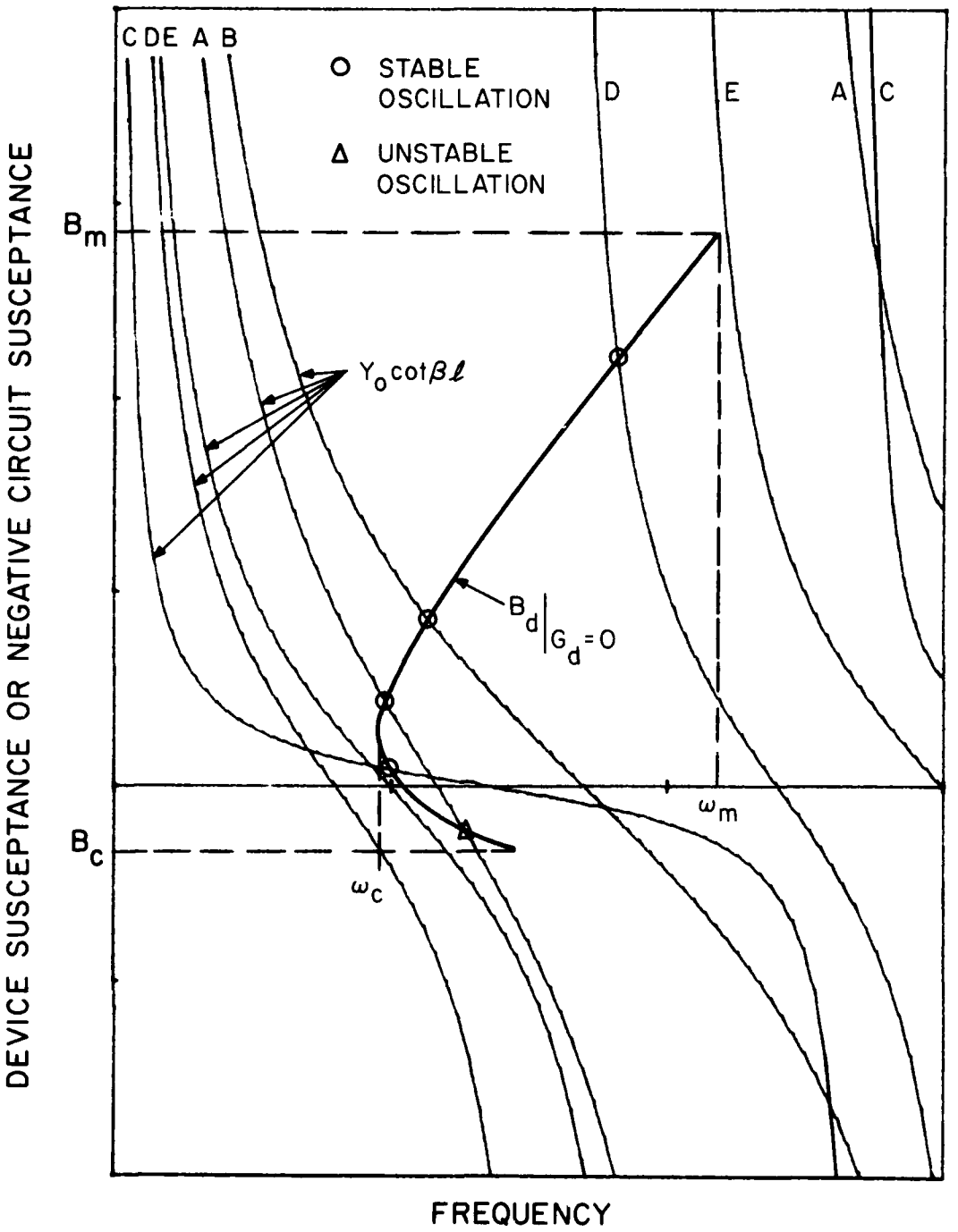


FIG. 4 DEVICE-CIRCUIT INTERACTION PERTINENT TO ROTATING MODE STABILITY SHOWING A TYPICAL $B_{dg}(\omega)$ PLOT [B_d FOR $G_d(V) = 0$] AND SEVERAL CIRCUIT NEGATIVE SUSCEPTANCES FOR THE TEM-LINE COMBINER. ONLY CIRCUIT CURVE E IS A STABLE SITUATION.

$Y_o \cot \beta\ell$. Dispersionless TEM lines are assumed. The maximum frequency of zero conductance is ω_m and the minimum frequency is ω_c. The end points of the B_{dg} curve correspond to solutions of Eq. 21a with $V = 0$ (small signal). Circuit functions A through D all result in solutions to Eq. 20 from improper selection of Y_o and/or line length ℓ. Only circuit admittance E will provide a stable situation. From Fig. 4 it is clear that stability can be avoided by choosing Y_o and ℓ such that

$$Y_o \cot \beta(\omega_c)\ell \overset{\leq}{\cong} B_c \tag{23a}$$

and

$$Y_o \cot \beta(\omega_m)\ell \overset{\geq}{\cong} B_m \quad , \tag{23b}$$

where B_c and B_m are defined in Fig. 4. Using B_c and ω_c as shown in Fig. 4 is sufficient in Eq. 23a but not always necessary as apparent from curve E. The best choice for B_c and ω_c depends on the nature of B_{dm} for the devices considered.

Conditions (23) can perhaps be visualized somewhat easier on the Smith chart as shown in Fig. 5, where $-B_{dg}/Y_o = -\overline{B}_{dg}$ is compared to $-\cot \beta\ell$. The circuit appears as a length of shorted TEM line and the angle $\theta(\omega)$ of its normalized admittance measured as shown is simply $2\beta(\omega)\ell$. Hence, stability requires that $\theta(\omega_c) \overset{\geq}{\cong} \arg(-\overline{B}_c)$ and $\theta(\omega_m) - 2\pi < \arg(-\overline{B}_m)$. This translates unambiguously to the stability conditions given by

$$\theta(\omega_c) \overset{\Delta}{=} \theta_c \overset{\geq}{\cong} \pi + 2\tan^{-1}(-\overline{B}_c) \tag{24a}$$

and

$$\theta(\omega_m) \overset{\Delta}{=} \theta_m \overset{\leq}{\cong} 2\pi - 2\tan^{-1}(-1/\overline{B}_m) \quad , \tag{24b}$$

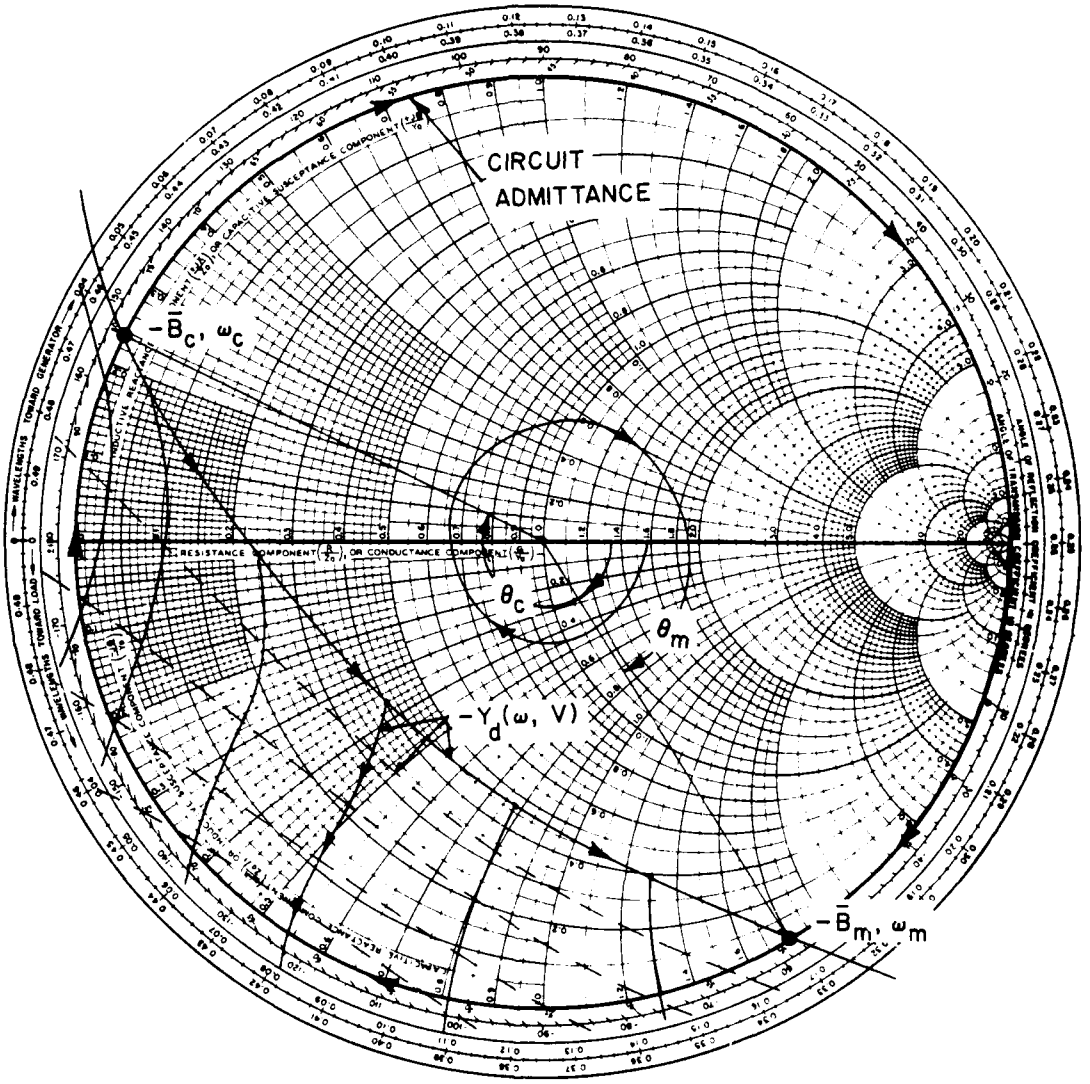


FIG. 5 STABILITY CONDITIONS INTERPRETED ON THE SMITH CHART SHOWING THE DEFINED ANGLES θ_c AND θ_m AND THE CIRCUIT ADMITTANCE.

where the $\tan^{-1}$ is either in the first or fourth quadrant. The line length ℓ determines the values of θ_c and θ_m and the normalization admittance scales the values of $\overline{B}_c$ and $\overline{B}_m$. An appropriate combination can often provide stability. Since β varies essentially linearly with frequency, it is apparent from Figs. 4 or 5 that the diode must have $\omega_m/\omega_c \simeq 2$ in order to satisfy Eq. 24.

Other solutions to Eqs. 23 are possible, and using the same arguments as for obtaining Eqs. 24 leads to conditions that

$$\left.\begin{aligned} \theta_c &\geqq (2n-1)\pi + 2\tan^{-1}(-\overline{B}_c) \qquad (25a) \\ \theta_m &\leqq 2n\pi - 2\tan^{-1}(-1/\overline{B}_m) \qquad (25b) \end{aligned}\right\} \quad n = 1,2,3,\ldots$$

or

$$\theta_c \leqq \theta_m \leqq -2\tan^{-1}(-1/\overline{B}_m) \quad . \qquad (25c)$$

Solutions to Eqs. 25a and b for $n > 1$ requires the diode active bandwidth to reduce such that $\omega_m/\omega_c \simeq 2n/(2n-1)$, but uses longer line lengths. Solution to Eq. 25c requires $B_m > 0$ and short line lengths but can accommodate large active bandwidths. Generally, the only practical solution turns out to be that available from Eq. 24, but it is interesting to consider the implications of Eq. 25 assuming IMPATT diodes having $B_c \cong 0$ and $B_m > 0$. With dispersionless lines so that $\theta_m = \alpha\theta_c$, where $\alpha = \omega_m/\omega_c$, then Eq. 25b gives

$$1 \leq \alpha \leq \frac{2n\pi - 2\tan^{-1} - \frac{1}{\bar{B}_m}}{\theta_c} \qquad (26)$$

which in combination with Eq. 25c gives the bandwidth-line-length limitations shown in Fig. 6. Maximum bandwidth occurs when $Y_o \to \infty$ or $\bar{B}_m \to 0$ in Eq. 26 which, of course, is not a practical limitation. It is clear that many-diode large-volume lossless combiners require diode band-limiting.

The greatest design flexibility is afforded through use of the stability conditions (Eqs. 24), and designs based on these relations will be treated in the rest of this section. Of course, Eqs. 24 must be satisfied for all reasonable values of RF voltage V, which can often be done as is shown by example. If ρ is defined as

$$\rho = \frac{B_c}{B_m} \quad , \qquad (27)$$

then for dispersionless lines, Eqs. 24 can be manipulated to give

$$\theta_c \geq \pi - 2\tan^{-1} \rho\bar{B}_m \qquad (28a)$$

and

$$\cot^{-1} \bar{B}_m + \alpha \tan^{-1} \rho\bar{B}_m \leq \frac{\pi}{2}(\alpha - 2) \quad . \qquad (28b)$$

For a diode with given α and ρ, the equality in Eq. 28b can be used

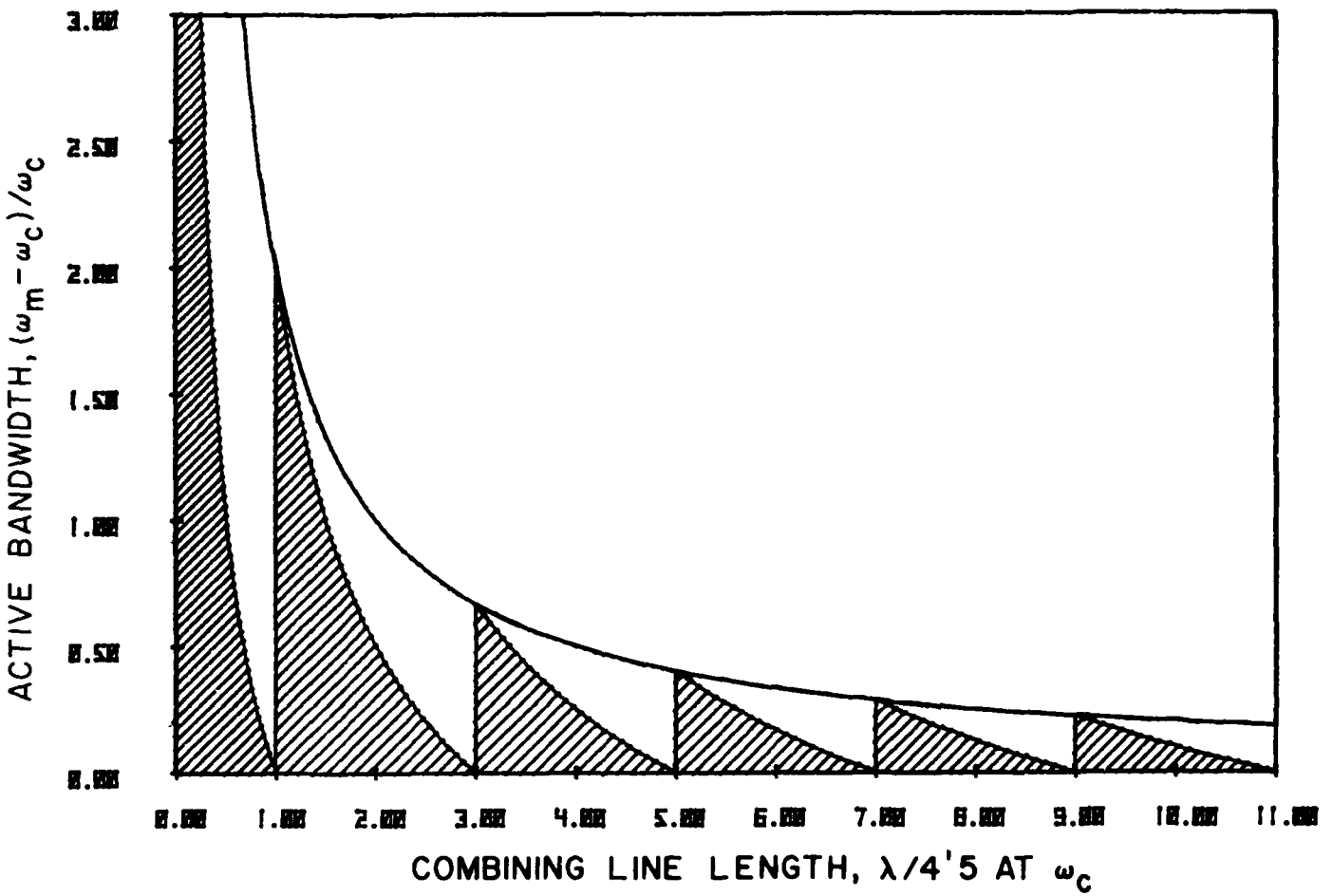


FIG. 6 ACTIVE DIODE BANDWIDTH LIMITATIONS REQUIRED AS A FUNCTION OF COMBINING LINE LENGTHS IN THE CIRCUIT OF FIG. 2 WHERE $B_c = 0$ AND $B_m > 0$ HAS BEEN ASSUMED.

to find a minimum value of $\bar{B}_m$ from which a value of $Y_o = B_m/\bar{B}_m$ can be determined. The equality in Eq. 28a then gives the required θ_c. Shown in Fig. 7 is a plot of $(2/\pi)\cot^{-1}\bar{B}_m$ as a function of α for various ρ values obtained from Eq. 28b. The graph has four sectors with the upper two corresponding to chip devices with $B_m > 0$. Typically silicon devices have $B_c < 0$ or $\rho < 0$, while GaAs devices have $\rho > 0$, the latter having greater design flexibility and less bandwidth limitation. Note that for silicon with $\rho < 0$, added shunt C improves stability, but at the obvious expense of diode Q and negative-resistance level. When using Fig. 7, it should be remembered that it represents the solution to the equality in Eq. 28b, and there can be diode cases where the inequality holds, providing stability margins.

Finally, by writing $\bar{B}_m$ as

$$\bar{B}_m = b_m A/Y_o \quad , \tag{29}$$

where A is the diode area and b_m is the susceptance per unit area, then if a maximum value of $\bar{B}_m = \bar{B}_{m,max}$ exists,

$$\left(\frac{A}{Y_o}\right)_{max} = \frac{\bar{B}_{m,max}}{b_m} \quad . \tag{30}$$

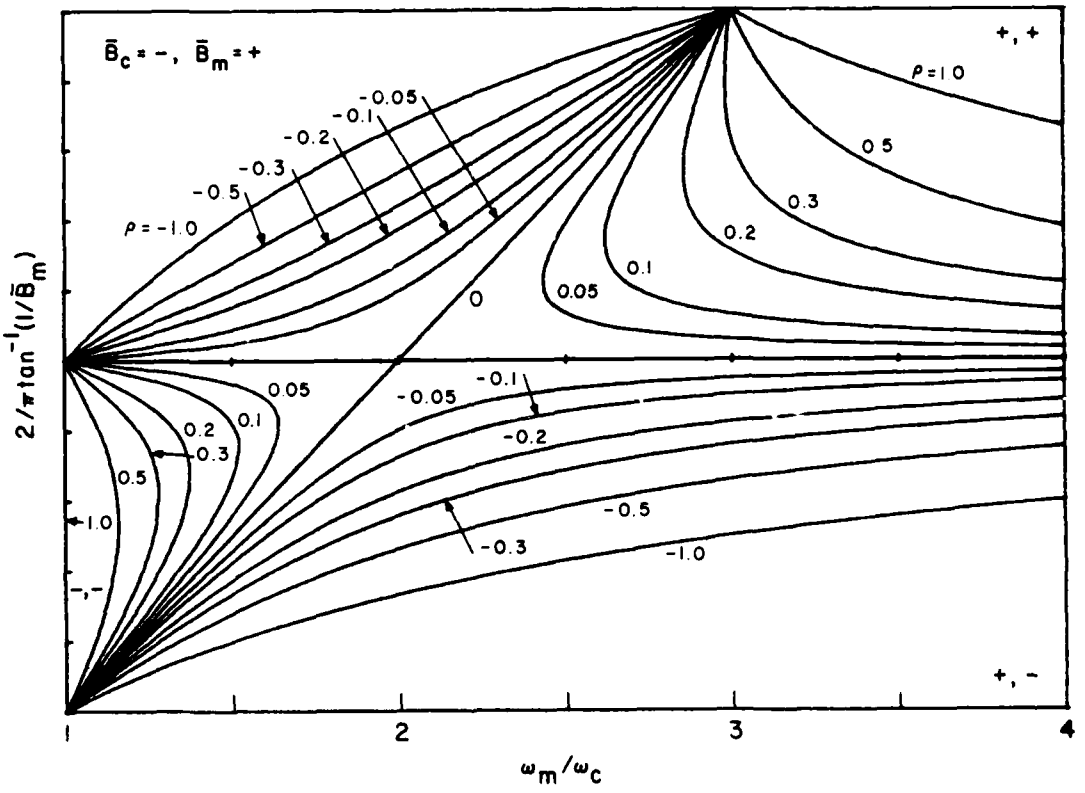


FIG. 7 LIMITATIONS ON THE VALUE OF $\bar{B}_m$ AS A FUNCTION OF ACTIVE BANDWIDTH WITH $\rho = B_c/B_m$ AS A PARAMETER. GREATEST DESIGN FLEXIBILITY OCCURS FOR $\rho > 0$ AND $\alpha = \omega_m/\omega_c < 2$.

Hence a maximum A/Y_o product for the diode combiner exists for stability reasons. In practice, the maximum area and power capability of the diode will be determined both by physical constraints on Y_o and thermal resistance as related to diode area.

Even-Mode Design Considerations. Within the confines imposed by the stability constraints above, certain considerations should be given to the even-mode oscillator or amplifier design. For the circuit of Fig. 2, each diode admittance will be rotated through the length of TEM line and added to N - 1 essentially identical admittances at the combining point. An equivalent circuit for this is shown in Fig. 8, assuming identical diodes. Practical considerations dictate that the total admittance level at the combining point should have reasonable values around the design frequency. Since adding together N diodes acts like an ideal impedance transformer, the optimum situation is to have the admittance real at the design frequency in an antiresonance mode. Again, the nature of the IMPATT admittance and the TEM line lengths required for mode stability can often allow this condition to be met, making realization of the desired load admittance Y_L straightforward.

Diode Design Considerations. The combining technique indicated here requires proper design of both diode and circuit. Circuit design flexibility is enhanced by using diodes which have active bandwidths $\omega_m/\omega_c \cong 2$ and optimum frequencies appropriate for simplified even-mode design. Fortunately, the design of IMPATT diodes and the technology for fabricating them has advanced to the point where the above device goals are likely achievable. With the proper doping profile and bias current density, ω_c, ω_m and the design frequency can be controlled to

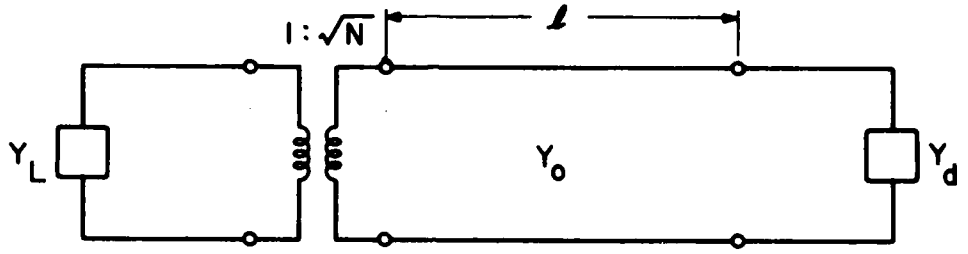


FIG. 8 AN EQUIVALENT CIRCUIT FOR THE N-DIODE TEM-LINE COMBINER FROM AN ADMITTANCE POINT. THE POWER IN Y_L IS N TIMES THE POWER GENERATED BY Y_d.

simplify combiner design. Examples of combiner design using this method are now given.

A Ten-Diode X-Band 25-W Microstrip Combiner. The admittance properties $Y_d(j\omega,V)$ of an X-band GaAs Read HI-LO IMPATT diode used for a design example are shown in Fig. 9. These characteristics were determined experimentally using large- and small-signal measurements and de-embedding techniques. For this diode, the dc bias current was 150 mA with a voltage of approximately 66 V under large-signal conditions. The optimum frequency and RF voltage level are at 9.5 GHz and 40 V, respectively, providing an output power of 2.64 W at approximately 27-percent efficiency.

As seen from Fig. 9, both B_m and B_c are positive and the active bandwidth $\omega_m/\omega_c < 2$, allowing substantial freedom in the choices of Y_o and ℓ for the combining lines. Appropriate choices for these parameters can thus be made so that the optimum power admittance for the diode viewed at the common combining point will lie on the real axis with a normalized admittance value less than unity. θ_d is defined as the angle in the reflection coefficient plane of the optimum normalized diode admittance, i.e.,

$$\tan \theta_d = \frac{2(-\overline{B}_{do})}{\overline{G}_{do}^2 + \overline{B}_{do}^2 - 1} , \qquad (31)$$

where $\overline{Y}_{do} = \overline{G}_{do} + j\overline{B}_{do}$ is the Y_o-normalized optimum power admittance at frequency ω_o. For the optimum admittance to rotate to the real axis at the combining point as shown in Fig. 10 requires that $\theta_d = (\omega_o/\omega_c)\theta_c - \pi$ or, using $\theta_c = \pi - 2 \tan^{-1} \rho\overline{B}_m$,

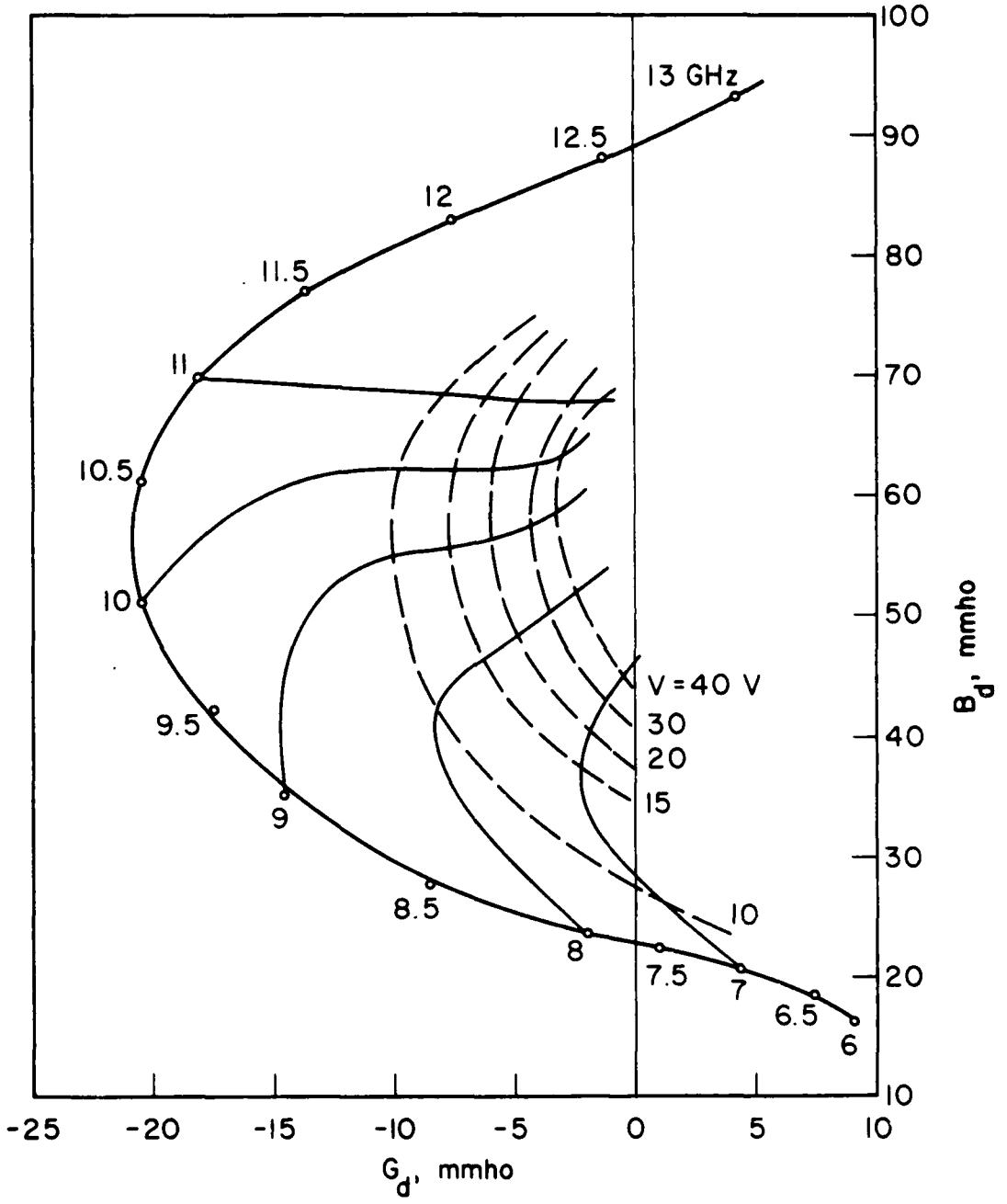


FIG. 9 ADMITTANCE CHARACTERISTICS OF AN X-BAND, 2.5-W READ-TYPE IMPATT DIODE AS DETERMINED EXPERIMENTALLY.

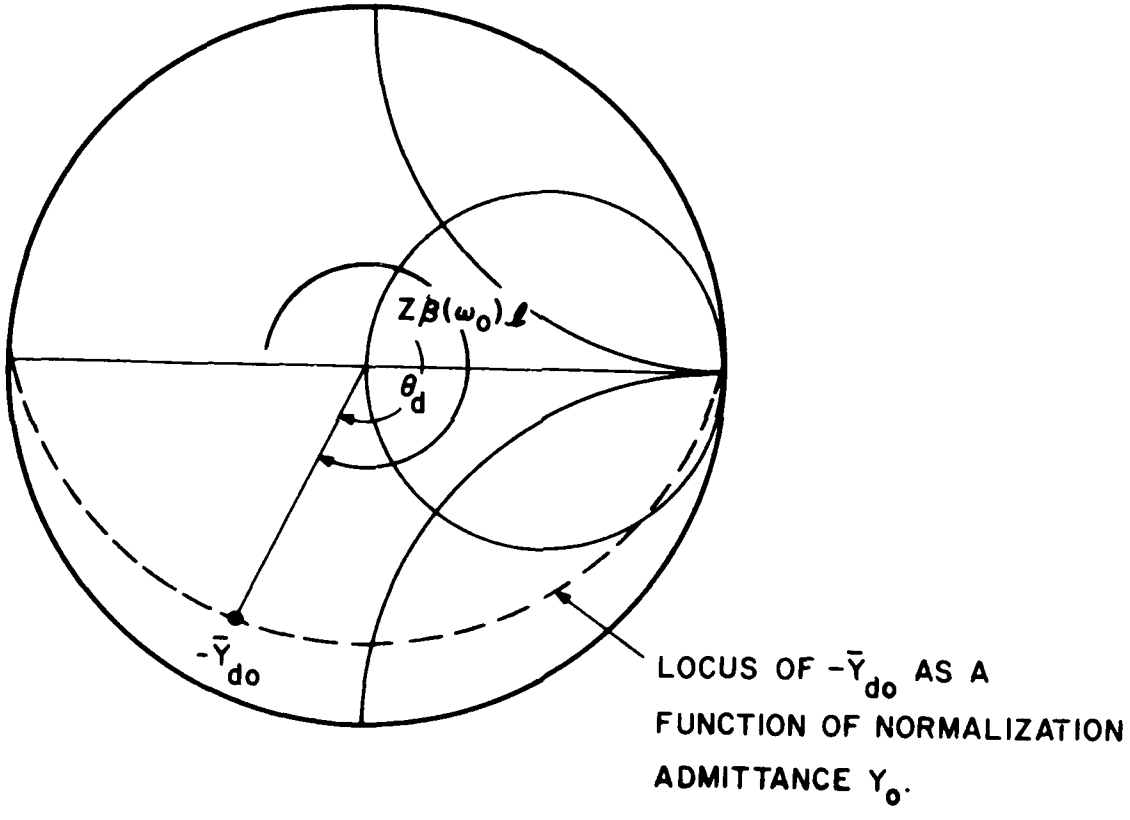


FIG. 10 CONDITIONS REQUIRED ON $-\bar{Y}_{do}$ FOR ROTATION TO THE REAL AXIS OF THE SMITH CHART AND SIMPLIFIED IMPEDANCE MATCHING.

$$\theta_d = \frac{\omega_o}{\omega_c}\left(\pi - 2\tan^{-1}\rho\bar{B}_m\right) - \pi \quad . \tag{32}$$

Combining Eqs. 32 and 31 and letting $Q_d = B_{do}/G_{do}$ gives

$$-\frac{2\bar{B}_{do}}{\bar{B}_{do}^2\left(1+\frac{1}{Q^2}\right)-1} = \tan\left\{2\pi - \frac{\omega_o}{\omega_c}\left[\pi - 2\tan^{-1}\rho\cdot\left(\frac{B_m}{B_{do}}\right)\bar{B}_{do}\right]\right\} \quad . \tag{33}$$

The optimum choice for θ_d is $\pi/2$ since this will maximize the reflection coefficient magnitude of $\bar{Y}_{do}$. However such a choice in this case would require the use of lines with unreasonably large values of Y_o. For this design, a choice of $Z_o = 1/Y_o$ of 35 Ω was used resulting in $\bar{B}_{do} = 2.14$, $\theta_c = 2.83$ and $\theta_d = 0.88$ with $\rho = 0.051$ and $\omega_c = 6.7$ GHz.

Shown on the Smith chart of Fig. 11 are the normalized diode admittance characteristics before and after rotation through the line to the combining point and the characteristics resulting from a ten-diode combiner. It should be clear why the optimum power point should lie on the real axis for simplest oscillator/amplifier design. Optimum oscillator performance at 9.5 GHz for the ten-diode combiner now requires a load admittance of $Y_L = 0.2$, $Y_o = 0.0057$, or $Z_L = 175$ Ω. This could easily be realized by using a $\lambda/4$ transformer from a 50-Ω output impedance level.

As a stable amplifier, this combiner would have very low gain since the normalized load admittance would have to be greater than 1.8 to avoid any oscillation, as can be seen from Fig. 11. However, the combiner could be used as an injection locked oscillator to provide maximum diode power capability with any desired locking gain. As an example

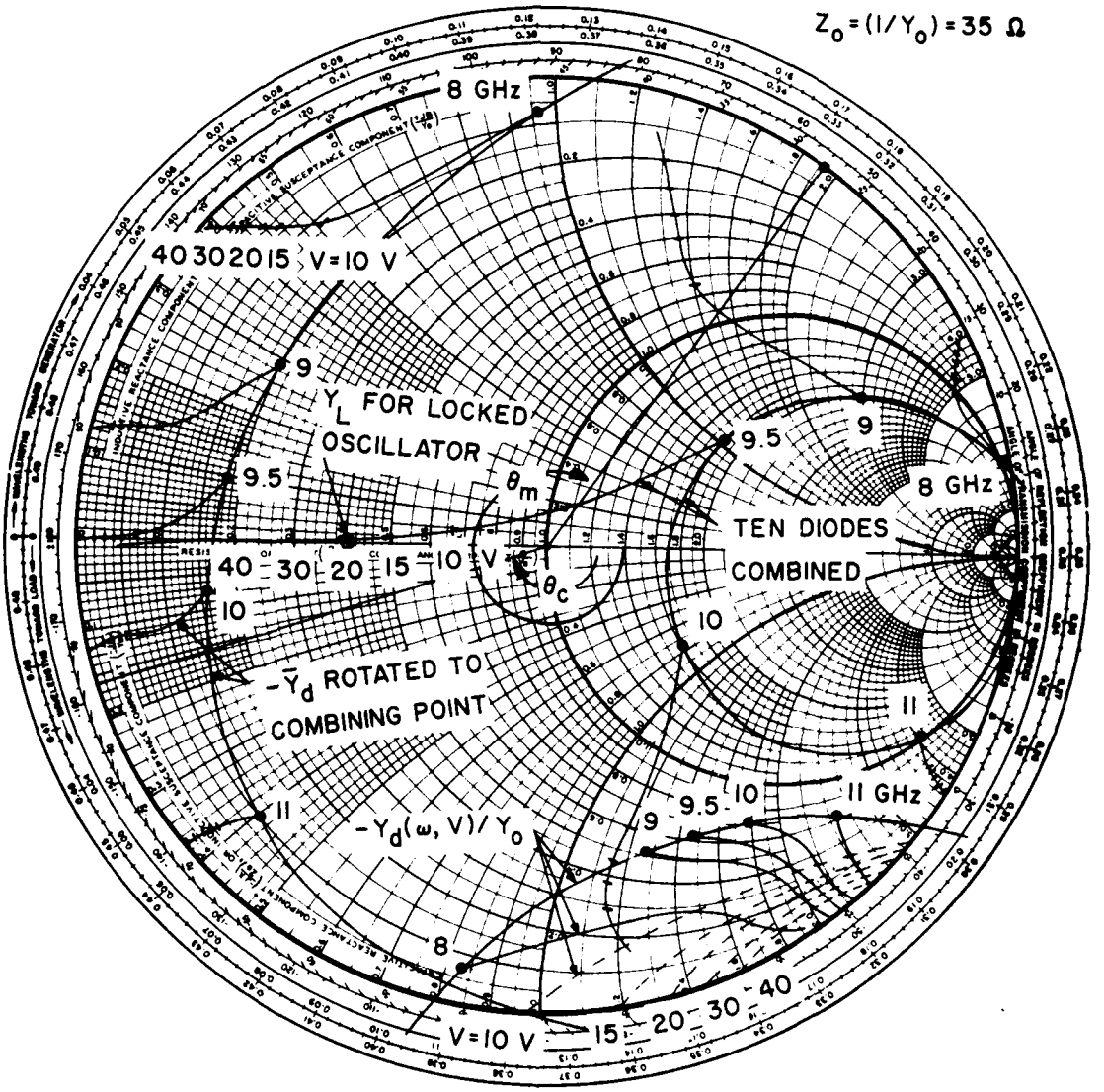


FIG. 11 NORMALIZED DIODE CHARACTERISTICS OF FIG. 9 BEFORE AND AFTER LINE ROTATION TO THE COMBINING POINT. ALSO SHOWN IS THE RESULT OF COMBINING TEN DIODES. THE VALUE OF $\bar{Y}_L$ CHOSEN WAS FOR A LOCKED OSCILLATOR GAIN OF APPROXIMATELY 10 dB AT 9.5 GHz FOR TEN DIODES.

of performance as a locked oscillator, a normalized load admittance of 0.4 was selected to achieve approximately 10 dB of locking gain at 9.5 GHz with an optimum input RF level of 3 W. The locking trajectory on the device curves as a function of frequency is shown in Fig. 12 from 9 to 10 GHz. This trajectory was obtained by graphically solving the locking equation

$$Y_d(j\omega_i, V) + Y_c(j\omega_i) = \frac{I_L}{V} \quad , \tag{34}$$

where Y_c is the circuit admittance seen by the diode and I_L is the equivalent locking source related to the injected power P_L by

$$|I_L(\omega_i)| = \sqrt{8G_c(\omega_i)P_L} \quad . \tag{35}$$

From the analysis, the predicted power vs. frequency response of the locked oscillator is indicated in Fig. 13 for a constant RF power input of 3 W. The peak output power is 30 W at 9.5 GHz with a 3-dB bandwidth of approximately 600 MHz.

A microstrip realization of the ten-diode combiner is shown in Fig. 14. In the analysis above, the effect of bond wires and the bias network needed were neglected. However, there is so much design margin with the diodes used that proper design of these elements will not affect rotating mode stability. Line lengths can be shortened appropriately to account for bonding lead inductance. Coupling among the various combiner lines will provide nondegenerate eigenvalues which will be shifted somewhat from the degenerate value. For the expected small coupling, this shift can be handled by the design margin.

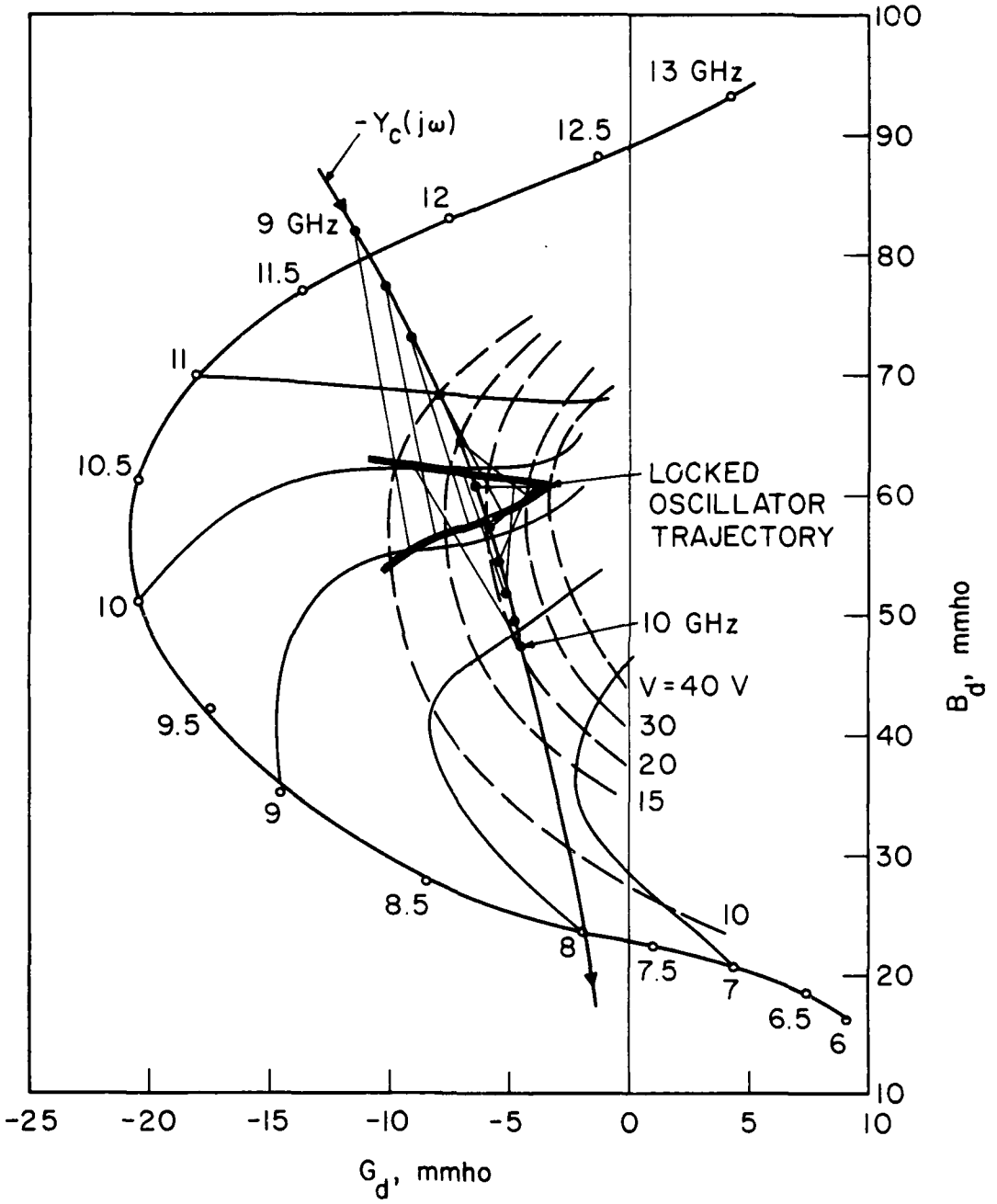


FIG. 12 DEVICE-CIRCUIT INTERACTION SHOWN IN DEVICE ADMITTANCE PLANE FOR THE X-BAND LOCKED OSCILLATOR. THE LOCKED OSCILLATOR TRAJECTORY IS ALSO SHOWN.

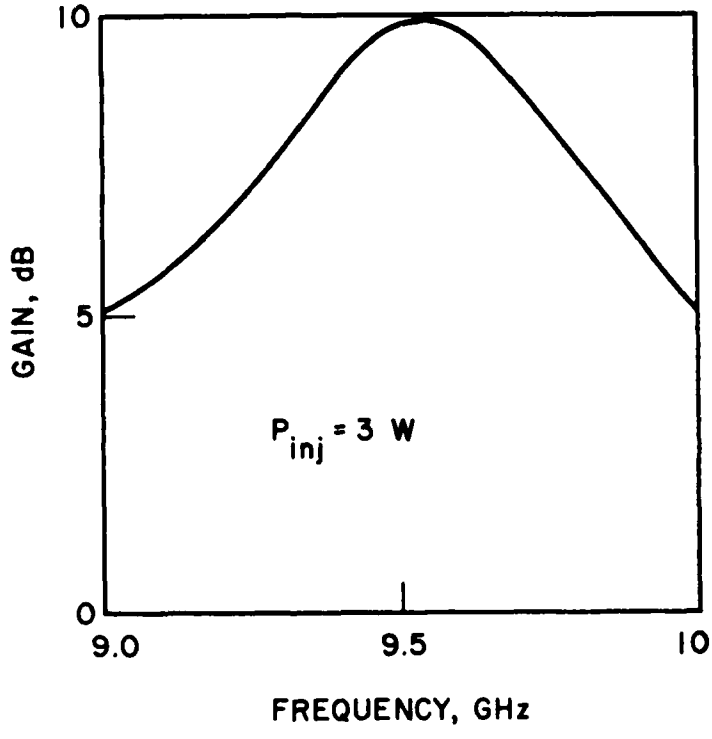
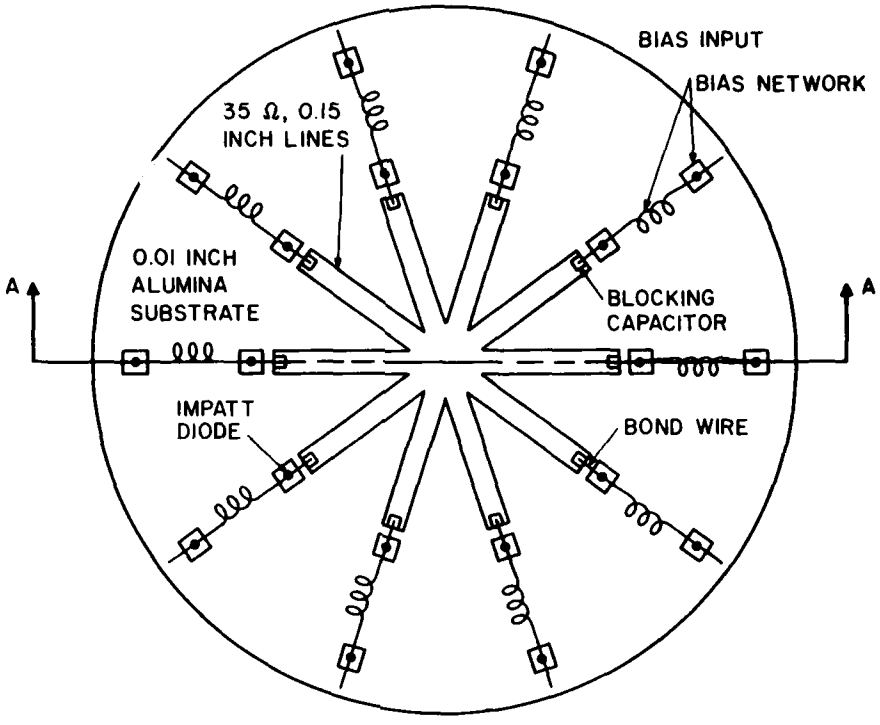
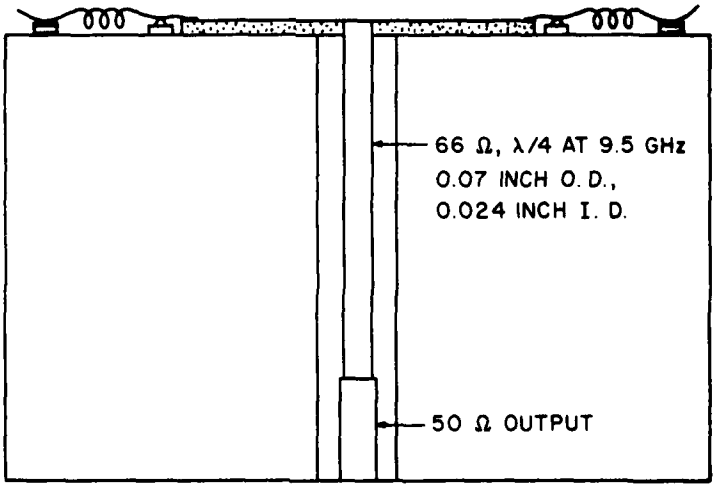


FIG. 13 LOCKED OSCILLATOR GAIN VS. FREQUENCY FOR THE X-BAND OSCILLATOR AT A CONSTANT RF LOCKING SIGNAL POWER OF 3 W. THE 1-dB BANDWIDTH IS ALMOST 300 MHz.



(a)



(b)

FIG. 14 A POSSIBLE MICROSTRIP REALIZATION OF THE TEM-LINE COMBINER OF FIGS. 12 AND 13.

A Millimeter-Wave Example. In this example, the properties of a millimeter-wave double-drift silicon IMPATT diode are used to develop the associated circuit design constraints. Realization of a symmetrical TEM-line combiner at millimeter wavelengths would likely require the use of millimeter-wave integrated circuit technology.

Shown in Fig. 15 are the admittance per unit area ($\mho/cm^2$) characteristics of a silicon millimeter-wave double-drift IMPATT diode at a current density of 30,000 A/cm^2 and temperature of 500°K. These properties were obtained using computer simulation programs developed at The University of Michigan.[13] This particular device is appropriate for operation in the 80- to 100-GHz frequency range. The maximum power generated by this IMPATT profile occurs at approximately 85 GHz and an RF voltage of V = 13 V and is 72.75 kW/cm^2.

The curves of Fig. 15 can be used to find the locus $b_{dg}(\omega)$, i.e., the curve of device susceptance at the RF voltage which makes $g_d(\omega,V) = 0$ (see Eqs. 21 and 22). This locus is shown in Fig. 16, indicating the typical double-valued behavior at the lower end of the active bandwidth from 53 to approximately 65 GHz. Based on this curve, it is possible to adjust the circuit admittance for the rotating modes to avoid intersection as in Eq. 23. Since the device is specified in terms of admittance per unit area, the appropriate line characteristic admittance will be normalized to the device area A_d. It is desirable to have the Y_o/A_d value as small as possible or, equivalently, the A_dZ_o product as large as possible, where $Z_o = 1/Y_o$. This allows a maximum area and RF power level for any given Z_o value. The stable solution indicated in Fig. 16 has $A_dZ_o = 1.33 \times 10^{-4}\ \Omega\text{-cm}^2$, with ℓ a quarter wavelength at 53 GHz (dispersionless lines assumed). This

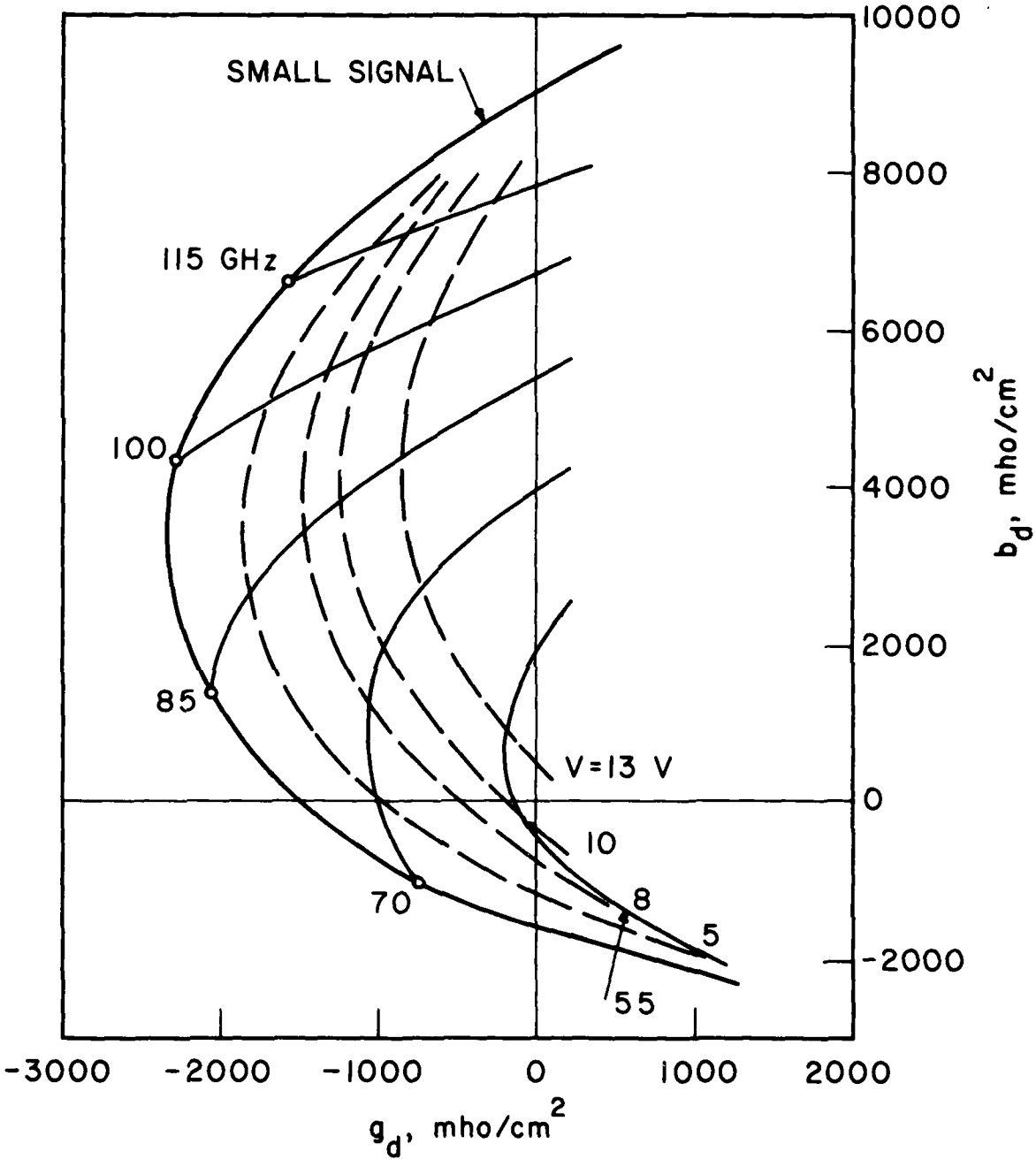


FIG. 15 THE CALCULATED ADMITTANCE CHARACTERISTICS PER cm^2 OF A MILLIMETER-WAVE DOUBLE-DRIFT SILICON IMPATT DIODE AT A DC CURRENT DENSITY OF 30,000 A/cm^2.

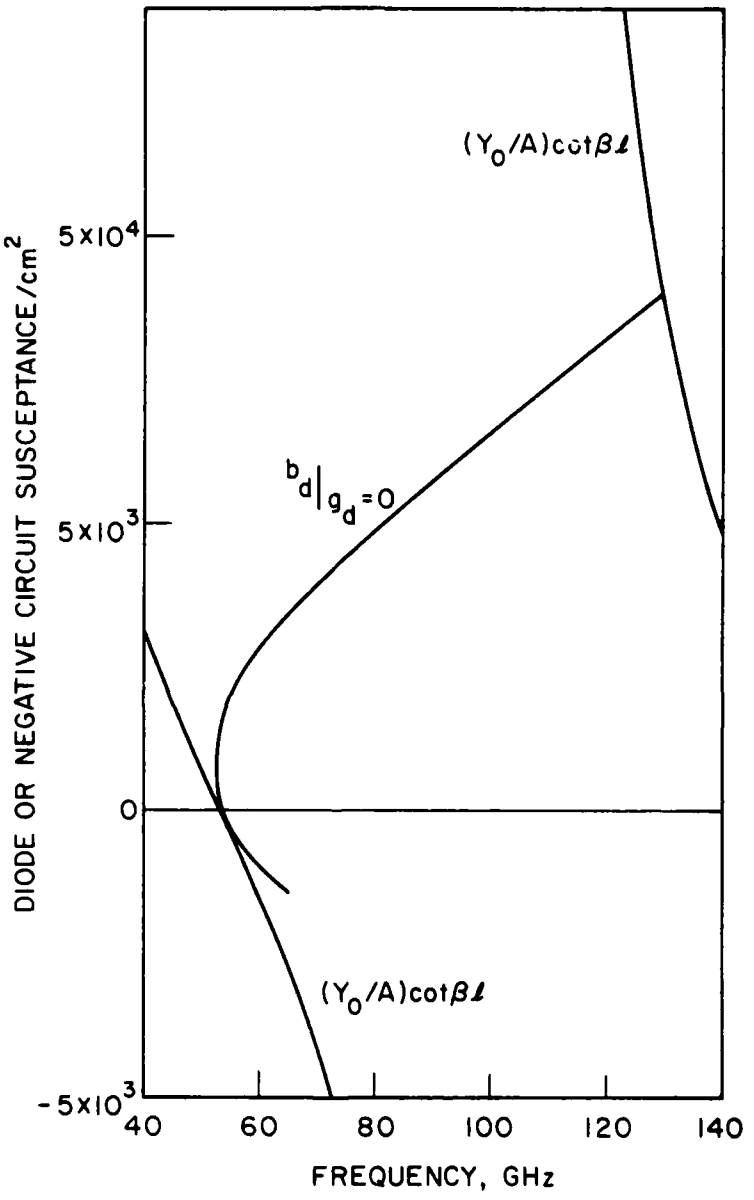


FIG. 16 THE LOCUS b_{dg} FOR THE CHARACTERISTICS OF FIG. 15 AND THE CIRCUIT NEGATIVE SUSCEPTANCE FOR A ROTATING-MODE-STABLE TEM-LINE SECTION. FOR THIS CASE, $A_d Z_o$ = 1.33 x 10^{-4} Ω-cm^2.

value of AZ_o gives a maximum diode power impedance product PZ_o = 9.68 W-Ω at approximately 85 GHz. The power impedance product is a useful parameter for comparing IMPATT diodes combined in this way.

Shown in Fig. 17 is the negative device admittance from Fig. 15 plotted on the Smith chart and normalized to the (Y_o/A_d) value given above. The combiner line length results in the maximum power negative device admittance at 87 GHz rotating to the real axis at the combining point to provide a normalized value of 0.08. Hence, for an N diode combiner oscillating at 87 GHz and maximum device power, Y_L would be chosen as

$$Y_L = 0.08\ NY_o,\ A_d/Y_o = 1.33 \times 10^{-4}\ \Omega\text{-cm}^2 \quad . \qquad (36)$$

For an injection locked oscillator, Y_L can be chosen larger than in Eq. 36 depending on the locking gain desired. A locking gain of 10 dB occurs for $Y_L \cong 0.16\ NY_o$.

The locked oscillator trajectory for the case of approximately 10 dB of locking gain at 87 GHz is shown on the device characteristics in Fig. 18. As with the previous example, this curve was found by a graphical solution to Eq. 34 while holding the injected power Z_o level constant at 1.15 W-Ω per diode. A curve of the locking gain vs. frequency is shown in Fig. 19 and it indicates a 3-dB bandwidth of approximately 15 GHz and a 1-dB bandwidth of nearly 9 GHz.

For this example, the value of Z_o was not specified but the value of AZ_o had a maximum value of $1.33 \times 10^{-4}\ \Omega\text{-cm}^2$. How this product is shared between A and Z_o depends on two factors in particular. The device area must be consistent with the associated thermal resistance to achieve normal operating temperatures, and there will be a lowest value

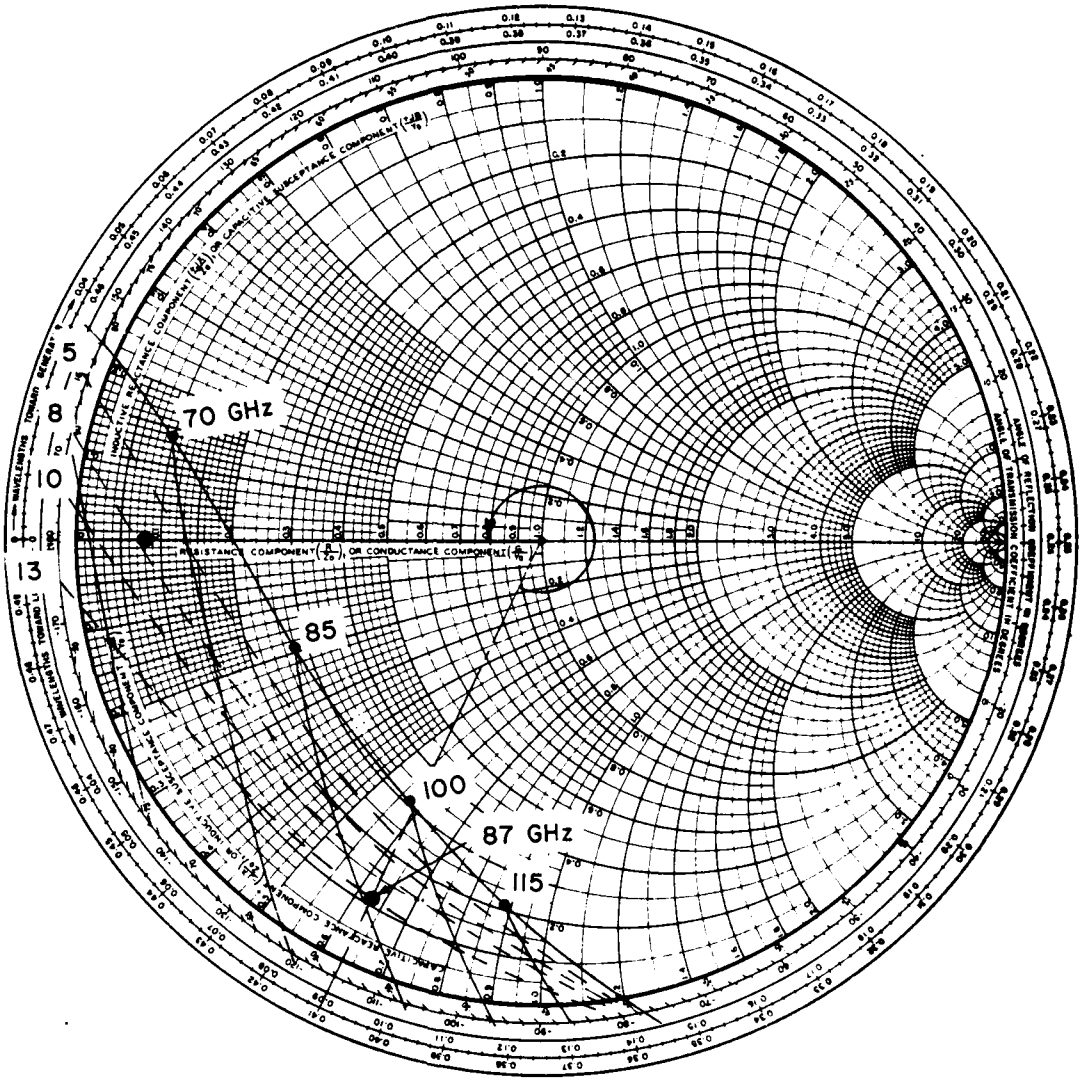


FIG. 17 THE ADMITTANCE CURVES OF FIG. 15 NORMALIZED TO Y_o/A_d AND PLOTTED ON THE SMITH CHART. THE MAXIMUM POWER ADMITTANCE AT 87 GHz MAPS TO A REAL VALUE AT THE COMBINING POINT.

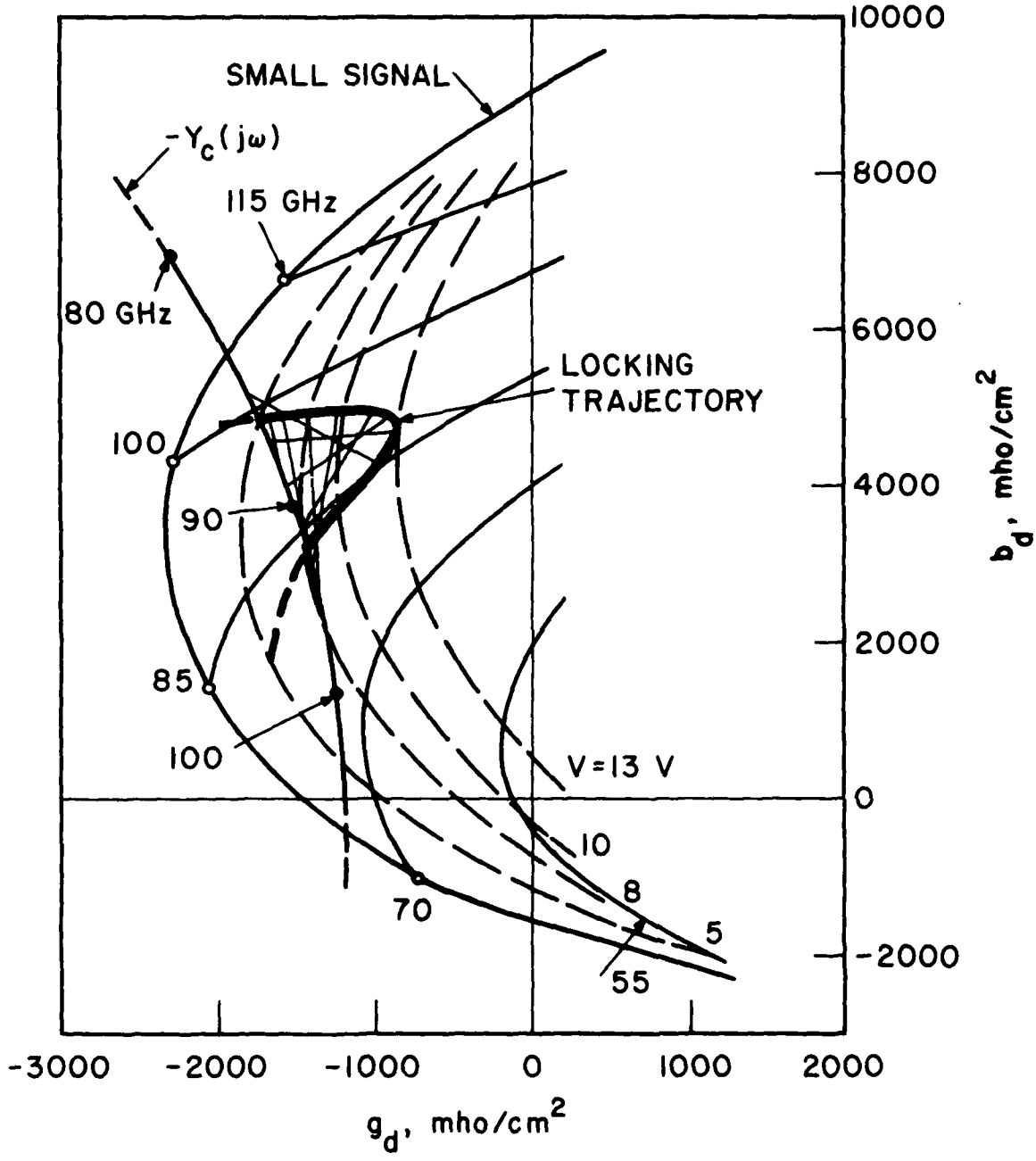


FIG. 18 DEVICE-CIRCUIT INTERACTION FOR THE EVEN COMBINING MODE SHOWING THE LOCKED-OSCILLATOR TRAJECTORY FOR Y_L SELECTED TO GIVE 10 dB OF LOCKING GAIN AT 87 GHz.

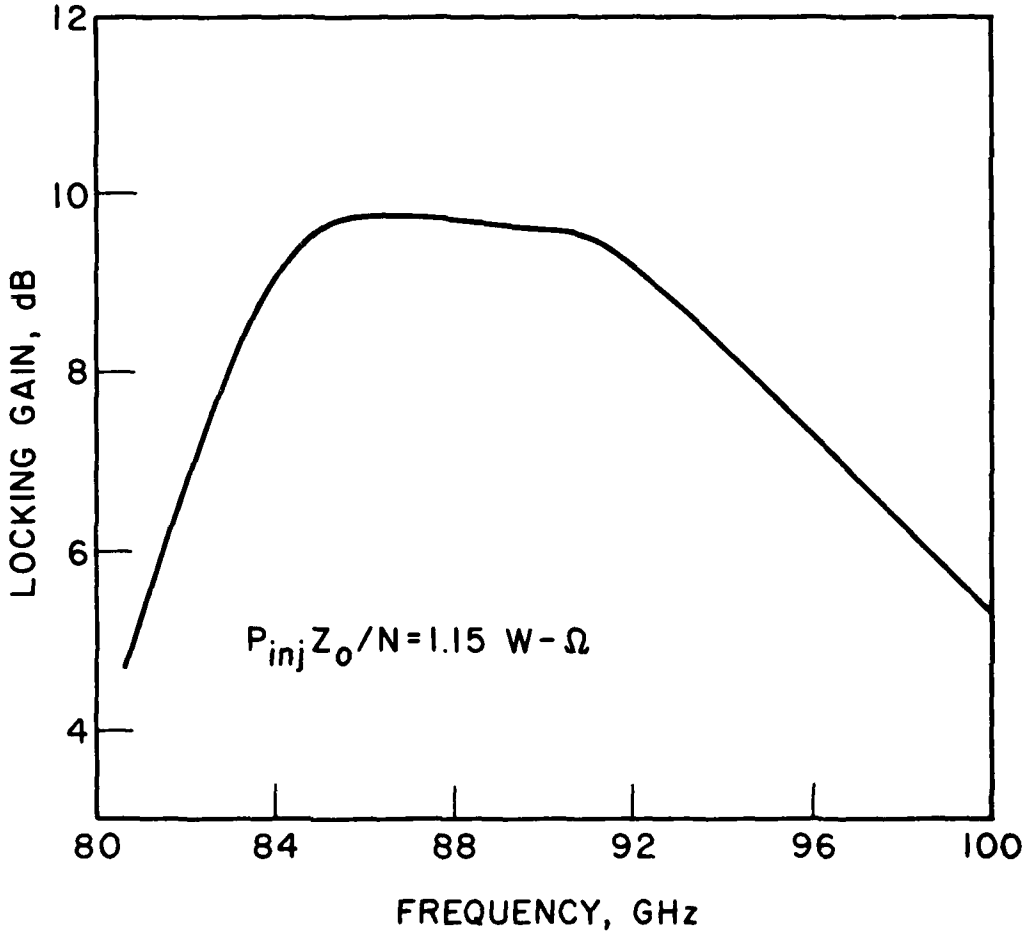


FIG. 19 LOCKED OSCILLATOR OUTPUT POWER VS. FREQUENCY OBTAINED FROM FIG. 18 FOR CONSTANT INJECTED POWER. IN THIS CASE, $P_{inj}Z_o/N$ = 1.15 W-Ω. A 1-dB BANDIWDTH OF APPROXIMATELY 9 GHz IS PREDICTED.

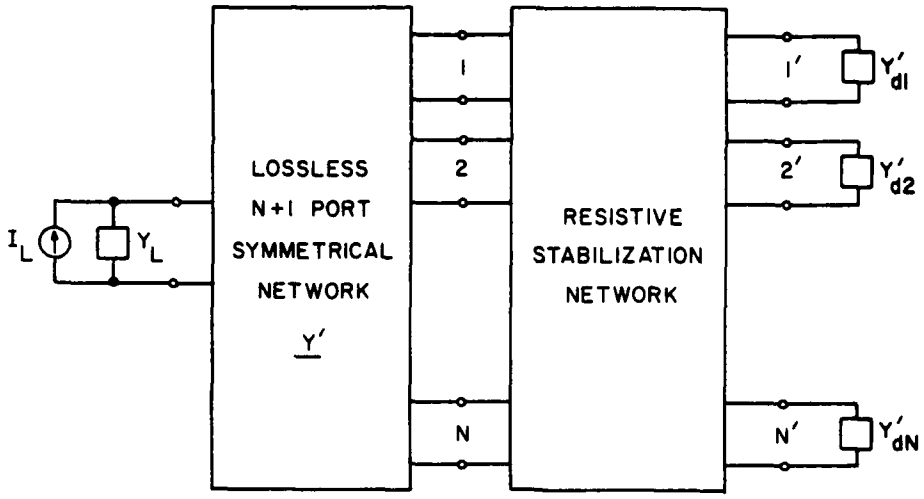
of Z_o for practical realization with the millimeter-wave integrated circuit technology. If Z_o = 20 Ω, for example, since PZ_o = 9.68 W-Ω per diode, the power added per device is approximately 0.5 W. Under pulsed conditions of high current density and higher device power per unit area, the PZ_o product will be much larger and this combining technique could provide substantial total power at reasonable Z_o values.

The AZ_o product or associated PZ_o product for a given device, such as the last example, can be increased by a two-section TEM line with appropriate levels of characteristic admittances and lengths. This technique is outlined in Appendix C with an example.

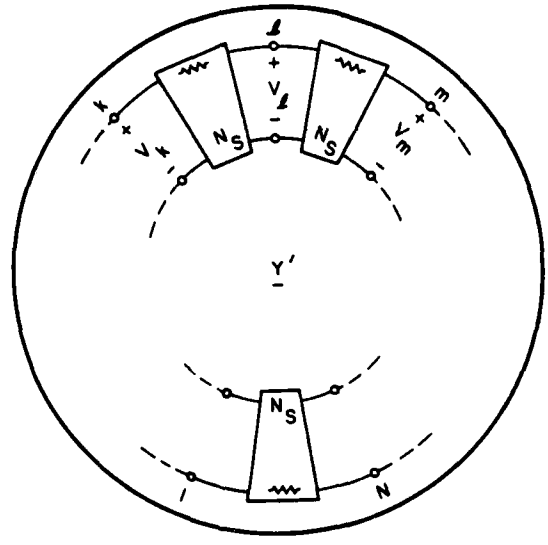
4. Resistive-Stabilized Radial-Symmetric Combiners

Circuit Description. Resistive stabilization networks embedded into the N+1-port diode power combiner can provide increased design flexibility over the lossless case while still retaining rotating mode suppression properties. The penalty is typically an increase in combiner size and stored energy to accommodate the stabilization with a corresponding reduction in combiner bandwidth. In addition, the circuitry becomes more complex, although the use of chip resistors and planar (microstrip) geometry results in fairly straightforward circuit designs.

Maximum advantage of resistive stabilization is possible if the circuit retains its symmetry properties as outlined in Section 2. The type of stabilization schemes utilized here are indicated in Figs. 20a and b. Basically, a lossless N + 1 port combiner is augmented by a symmetrical resistive stabilization network as in Fig. 20a. The use of primed diode admittances indicates that the diodes may be themselves embedded in a lossless network before stabilization occurs. In Fig. 20b,



(a)



(b)

FIG. 20 (a) A GENERAL RESISTIVE STABILIZATION NETWORK ADDED TO A SYMMETRICAL LOSSLESS N + 1 PORT COMBINER. THE PRIMED ADMITTANCES INDICATE POSSIBLE LOSSLESS CIRCUIT TRANSFORMATIONS. (b) THE FORM OF THE STABILIZATION NETWORKS IN (a) WHICH WILL BE CONSIDERED. RADIAL SYMMETRY IS ASSUMED.

the form of the stabilization network is given showing the use of identical two-port, symmetrical, lossy networks N_s sequentially connected from port to port of the lossless combining network of Fig. 20a. Such stabilization could easily be implemented in radial-symmetric planar networks. The properties of these networks can be specified so that all rotating modes are suppressed by resistive loading, while even-mode combining remains lossless.

Stabilization Networks and Combiner Eigenvalues. The form of the stabilization does not change the symmetry properties of the combining network and the eigenvectors of the new network will remain unchanged. The eigenvalues will, however, be modified by the presence of N_s and the new eigenvalues λ_n', $0 \leq n \leq N - 1$ can easily be found by several methods.

With reference to Fig. 20b, the equivalent circuit model used at the sequential combiner ports k, ℓ, and m for eigenvector or mode n is shown in Fig. 21a. It is required that the port-to-port networks be symmetrical and λ_n is the nth eigenvalue of the lossless, unstabilized combiner network. Furthermore, the stabilization network is assumed to be of the form indicated in Fig. 21b, where G_s represents a stabilization conductance (chip resistor) placed symmetrically between mirror image lossless networks. These networks from combiner port to the stabilization resistor are characterized by the Y-matrix $\underline{Y}_b$ given by

$$\underline{Y}_b = \begin{bmatrix} y_{aa} & y_{ab} \\ y_{ab} & y_{bb} \end{bmatrix} , \qquad (37)$$

which is not necessarily symmetrical.

The new eigenvalues can now be found from the requirement that

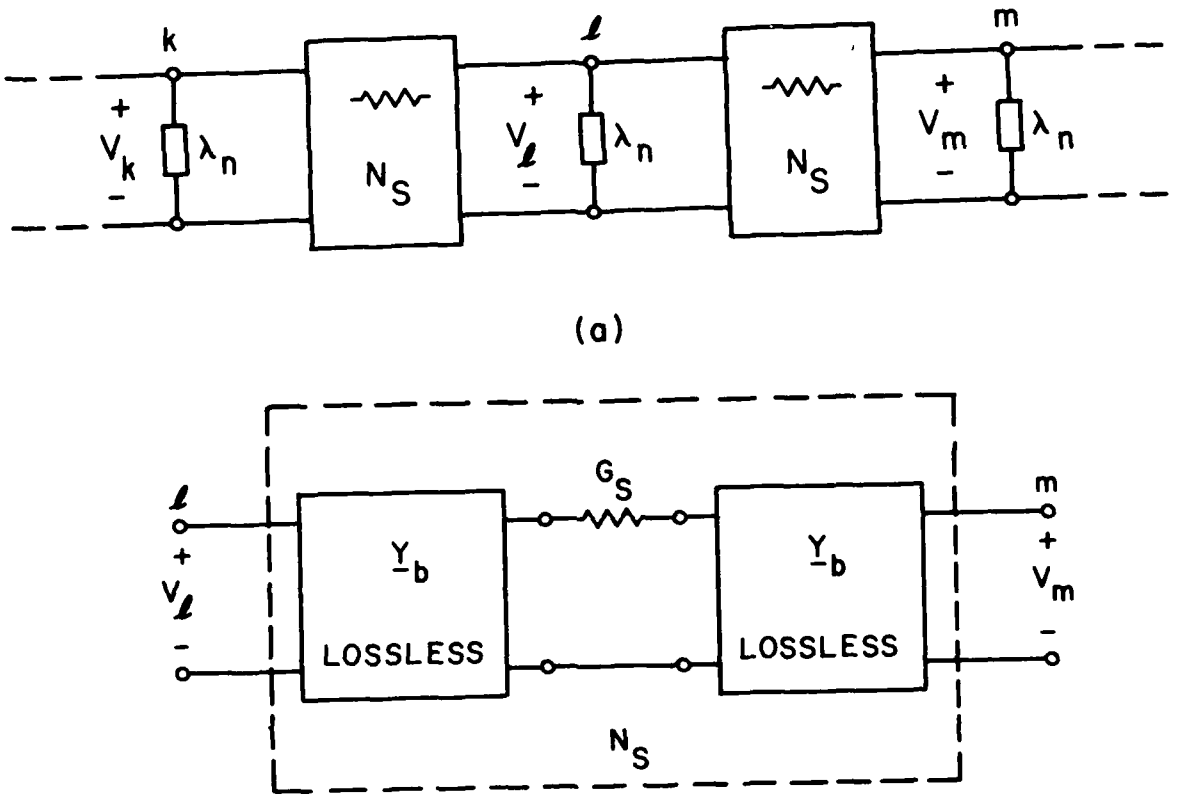


FIG. 21 (a) THE EQUIVALENT CIRCUIT MODEL AT THE PORTS k, ℓ, AND m FOR EIGENVECTOR OR MODE n OF THE SYMMETRICAL COMBINER. λ_n IS THE CORRESPONDING EIGENVALUE FOR THE LOSSLESS COMBINER PORTION. (b) THE FORM ASSUMED FOR THE PORT-TO-PORT STABILIZATION NETWORKS N_s OF (a). THE NETWORKS $\underline{Y}_b$ ARE LOSSLESS AND MIRROR IMAGES.

$$V_k = e^{-jna} V_\ell \tag{38a}$$

and

$$V_\ell = e^{-jna} V_m \quad . \tag{38b}$$

Analysis of the circuit of Fig. 21a with decomposition as in Fig. 21b with the voltage constraints above shows that λ_n' is given by

$$\lambda_n' = \lambda_n + Y_{ns} \quad , \tag{39}$$

where

$$Y_{ns} = 2\left[y_{aa} - \frac{y_{ab}^2}{y_{bb}} + \frac{y_{ab}^2}{y_{bb}} \frac{G_s(1 - \cos na)}{y_{bb} + 2G_s}\right] \quad . \tag{40}$$

As expected, for the zeroth (even) mode, Y_{os} is just twice the open circuit admittance of the lossless network $\underline{Y}_b$ which is purely imaginary. Of course λ_o is a positive real admittance since this is the combining mode. For all the rotating modes, $\mathrm{Re}\{\lambda_n\} = 0$ but $\mathrm{Re}\{Y_{ns}\} > 0$ because of G_s, and stabilization of these modes is possible with the proper selection of G_s and $\underline{Y}_b$ so that

$$Y_d'(j\omega, V) + \lambda_n'(j\omega) = 0 \tag{41}$$

is not satisfied for any ω, V where the diode is active.

TEM-Line Stabilization Networks. A case of practical interest is to have $\underline{Y}_b$ be represented by a TEM line of length ℓ_s and characteristic admittance Y_s so that

$$y_{aa} = y_{bb} = -jY_s \cot \beta\ell_s \tag{42a}$$

and

$$y_{ab} = \pm jY_s \csc \beta\ell_s \quad . \tag{42b}$$

Use of Eq. 42 in Eq. 40 shows that

$$G_{ns} = \mathrm{Re}\{Y_{ns}\} = 2G_s(1 - \cos na)\frac{1 + \tan^2 \beta\ell_s}{1 + \left(\frac{2G_s}{Y}\right)^2 \tan^2 \beta\ell_s} \quad . \tag{43}$$

As a function of frequency, G_{ns} oscillates between minimum and maximum values occurring when $\beta\ell_s$ takes on integral values of $\pi/2$. Simplified design for mode stability is possible if G_{ns} is made independent of frequency by choosing

$$\frac{2G_s}{Y_o} = 1 \tag{44}$$

so that

$$G_{ns} = 2G_s(1 - \cos na) \quad . \tag{45}$$

Stability of mode n is then accomplished simply by having

$$G_{ns} > -G'_{d,min} \quad , \tag{46}$$

where $G'_{d,min} = \min\{\mathrm{Re}[Y'_d(j\omega,V)]\}$ or the diode minimum negative conductance. Using Eq. 46 in Eq. 45 requires

$$G_s > -\frac{G'_{d,min}}{2(1 - \cos na)} \quad , \tag{47}$$

which must hold for all rotating modes. The worst case occurs when $na = \pm 2\pi/N$ ($n = 1$ or $N - 1$) requiring

$$G_s = \frac{Y_s}{2} > -\frac{G'_{d,min}}{2\left(1 - \cos\frac{2\pi}{N}\right)} \tag{48}$$

for overall stability.

In order to make use of realizable line admittance values Y_s, the diode admittance Y_d may have to be transformed through a low-loss network to Y_d' such that Eq. 47 can be satisfied in a practical fashion. In such a transformation, the number of diodes N is also a factor.

For the desired even mode, the stabilization network results in two parallel open circuit stubs across the (transformed) diode of length ℓ_s and characteristic admittance Y_s. The length of these lines can be used effectively in combination with the rest of the circuit for tuning and impedance matching purposes in the even-mode combiner circuit design.

A Ten-Diode 100-W X-Band Combiner. For this example, the IMPATT devices with characteristics shown in Fig. 3 were again used except each diode was assumed to be four times as large. Therefore, the admittance of the device would be scaled (increased) by four as would the RF power capability, providing 10 W per diode. The size increase could be obtained by doubling the diode diameter if the associated thermal resistance was consistent, or more likely by using a diode "quad." With such a large device and the resulting low impedance level, the lossless TEM combiner becomes impractical or unrealizable. It is impractical because with chip devices the line impedances required would be too low to realize effectively, and if a low-loss impedance transformer is used on the chip, the resulting increased reactance variation makes rotating mode stability difficult or impossible. Hence, a stabilized design is required for a reasonable and realizable solution for the combiner.

The low impedance level of the diode dictates a low-loss L-C impedance level transformation near the diode for matching purposes, at some expense in bandwidth. In addition, at the stabilization point,

the peak negative conductance of the transformed diode must relate to the stabilization line admittance Y_s as in Eq. 48, i.e.,

$$- G_{d,min} < Y_s\left(1 - \cos\frac{2\pi}{N}\right) = Y_s \quad , \quad (N = 10) \quad , \quad (49)$$

where Y_s represents a practical admittance level (~0.02 $\mho$). To satisfy Eq. 49 with $Y_s \approx 0.02$ $\mho$, the circuit of Fig. 22a was assumed and the package parasitics and line parameters were adjusted such that $-G_{d,min}$ occurred at the design frequency of 9.5 GHz. Bonding inductance and blocking capacitance are modeled by L_B and C_B, although their effect is minimal. The parameter values used are indicated in Fig. 22a.

The stabilizing line lengths were selected to provide a parallel resonance at 9.5 GHz, and the resulting admittance was mapped through a half-wavelength line at 9.5 GHz to the combining point. Hence, the total admittance at the combining point adds to a reasonable and realizable value. The negative admittance of the active device at the stabilization point, including the effect of the stubs, is shown on the Smith chart plot of Fig. 23. The equivalent circuit for the combiner is shown in Fig. 22b, and a possible microstrip realization is given in Fig. 24. Bias circuit elements indicated in Fig. 24 were assumed negligible in the analysis. It may be necessary to use the "bias circuit" elements for subharmonic suppression by providing a series resonance at the half frequency in addition to a high impedance at 9.5 GHz. The value of Y_L indicated was chosen for 10 dB of locking gain at 9.5 GHz.

Shown in Fig. 25 are the device admittance curves, the circuit admittance $Y_c(j\omega)$ and the locked oscillator trajectory for a peak

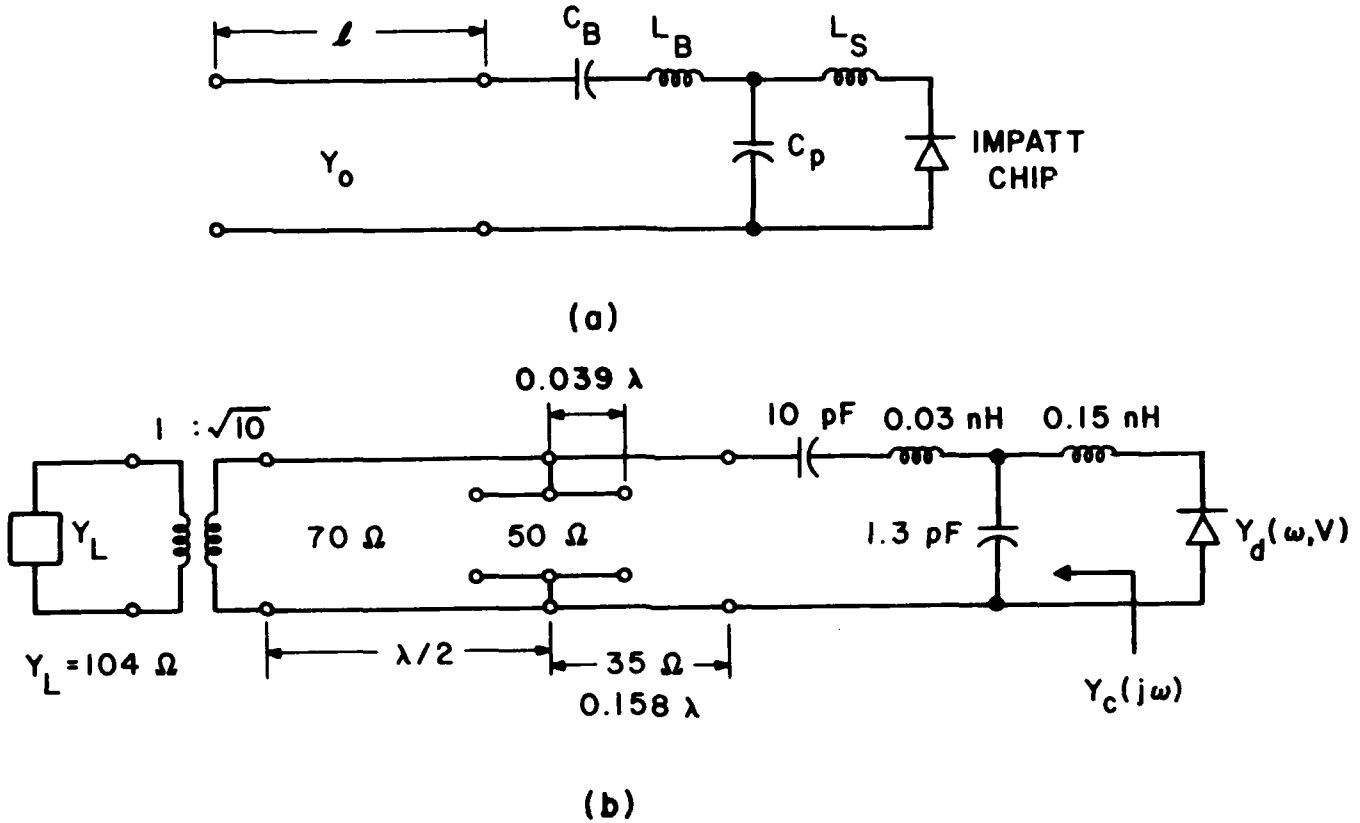


FIG. 22 (a) IMPEDANCE TRANSFORMATION USED TO OBTAIN Y'_d AT THE TERMINALS OF THE STABILIZATION NETWORKS. THE DIODE ADMITTANCE PROPERTIES ARE SHOWN IN FIG. 3 EXCEPT THE SCALES ARE INCREASED BY A FACTOR OF FOUR. (b) EQUIVALENT CIRCUIT FOR THE RESISTIVE STABILIZED TEN-DIODE COMBINER IN THE EVEN MODE WHERE THE STABILIZATION RESISTANCES ARE INVISIBLE. FOR THIS COMBINER, G_s = 0.01 ℧.

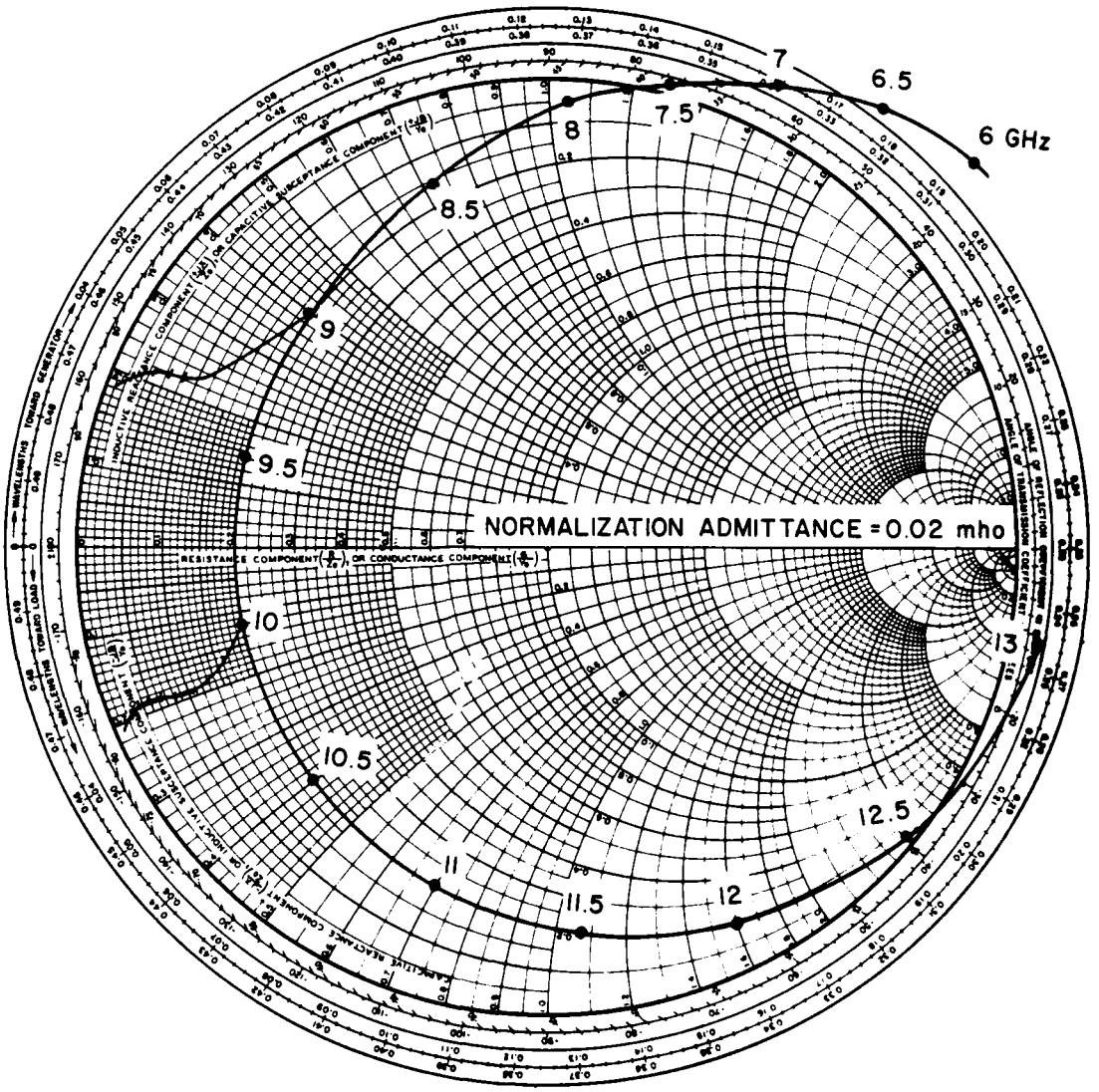
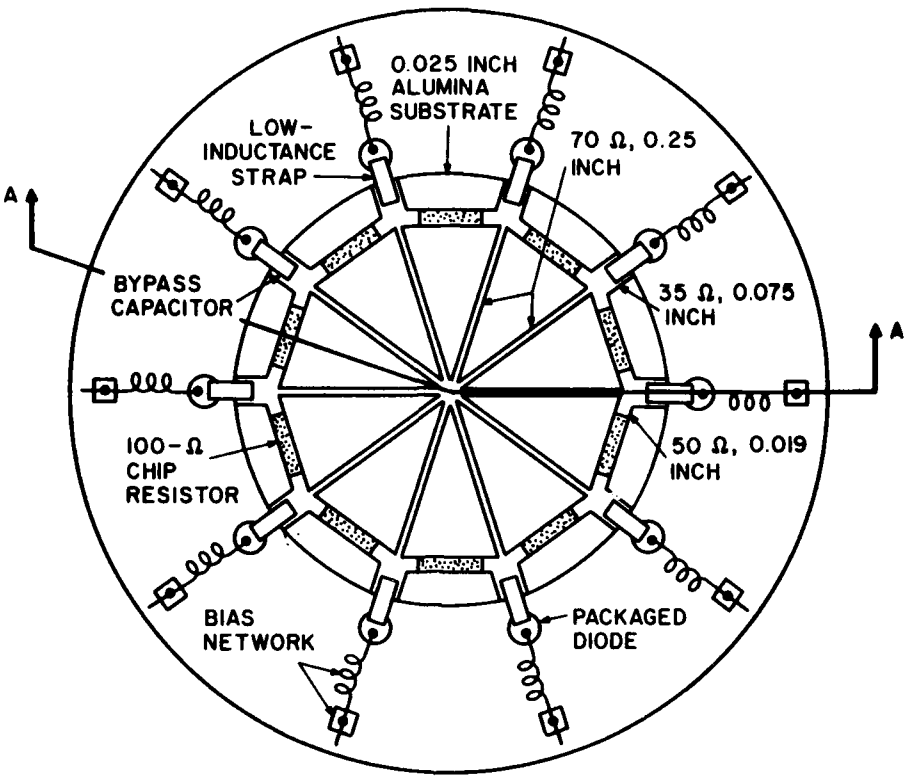
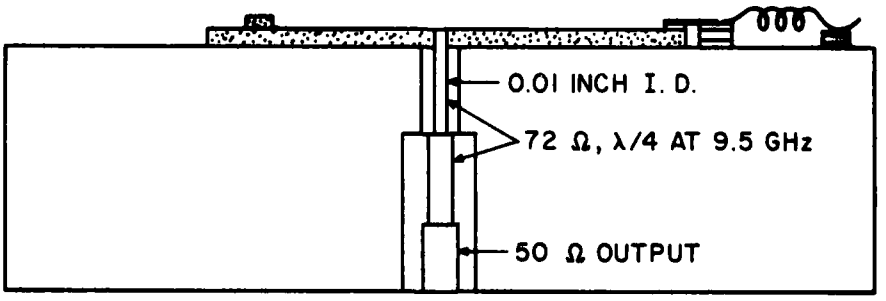


FIG. 23 THE DIODE ADMITTANCE PROPERTIES ROTATED TO THE COMBINING POINT WHERE THE CIRCUIT IS AS SHOWN IN FIG. 22b. THE ADMITTANCE IS RESONANT AT APPROXIMATELY 9.5 GHz.



(a)



(b)

FIG. 24 A POSSIBLE MICROSTRIP CIRCUIT REALIZATION OF THE COMBINER OF FIG. 22b INCLUDING THE USE OF PACKAGED DEVICES WITH PROPER PARASITICS AND BIASING NETWORKS.

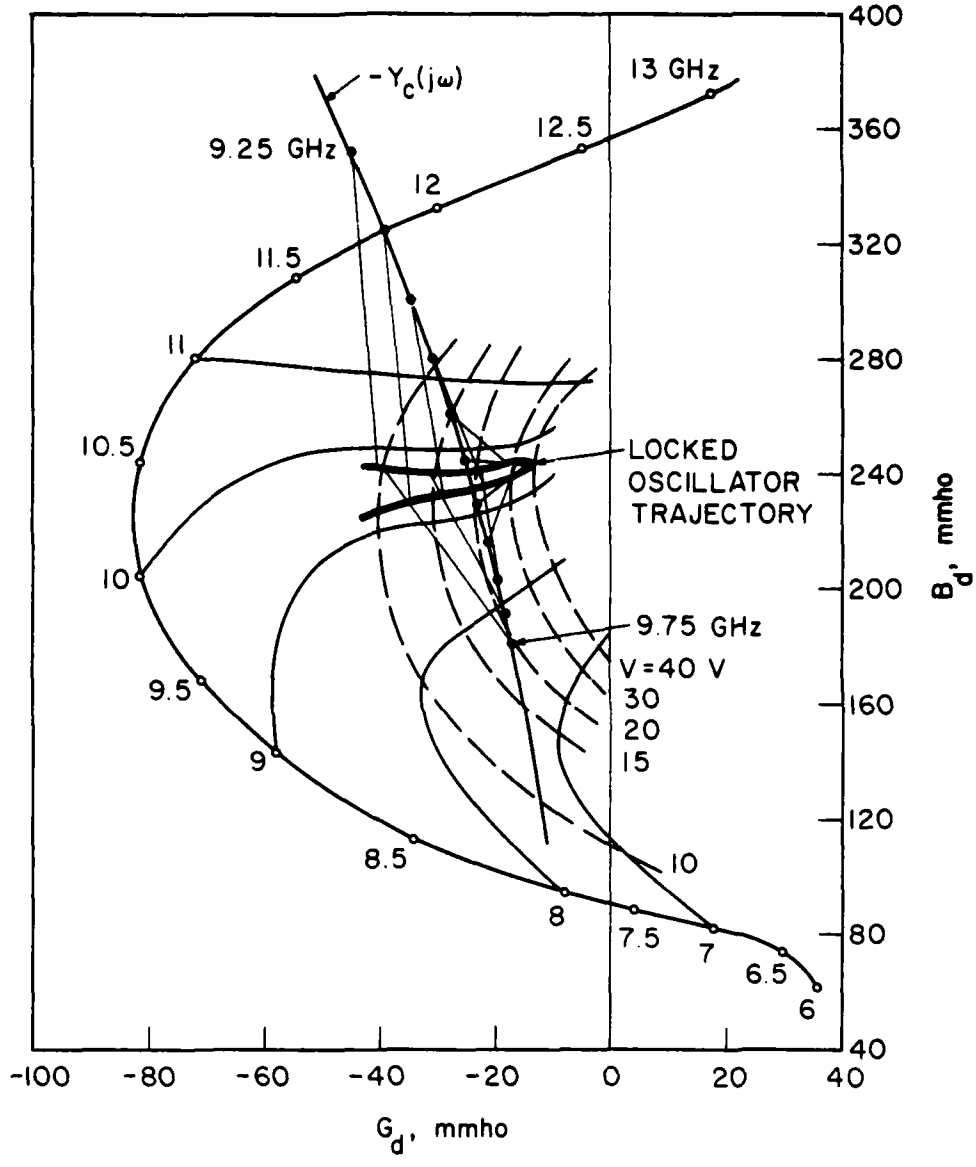


FIG. 25 DEVICE-CIRCUIT INTERACTION FOR THE CIRCUIT OF FIG. 22b WITH Y_L ADJUSTED FOR 10 dB OF LOCKED OSCILLATOR GAIN AT 9.5 GHz. THIS PLOT CAN BE COMPARED TO THAT OF FIG. 13.

locking gain of 10 dB at 9.5 GHz and maximum RF power. The bandwidth reduction from the previous lower power lossless design is apparent.

Total combiner output power as a function of frequency is shown in Fig. 26, indicating a peak output level of 117 W at 9.5 GHz and 10-dB gain. As before, the injected power level was held constant across the band, in this case being 11.3 W. The 3-dB bandwidth is approximately 270 MHz.

5. Summary and Conclusions

The combining circuits studied in this report differ from other designs primarily because the circuit design is more heavily constrained by the device properties. In this sense, the "device" and "circuit" are not separate entities, but are "matched" to each other's properties to optimally perform the power adding function. Combiners studied were of two basic types: lossless, radially symmetric TEM-line circuits and resistive stabilized, symmetric TEM-line combiners. In the former case, combiner even-mode stability required certain device and circuit properties which, when achieved, led to small size, low stored energy, potentially high-power combiners at both microwave and millimeter-wave frequencies as shown by 10-GHz and 90-GHz examples. Such combiners are ideally suited to integrated circuit techniques. Resistive stabilization of the combiner circuit is required for use with packaged devices or in the case of large active device bandwidths in order to achieve stability. For the symmetrical circuit case, a simple technique is available for determining the value and location of stabilization resistors which suppress odd modes but are invisible to even modes. An example of a high-power, x-band stabilized combiner was given.

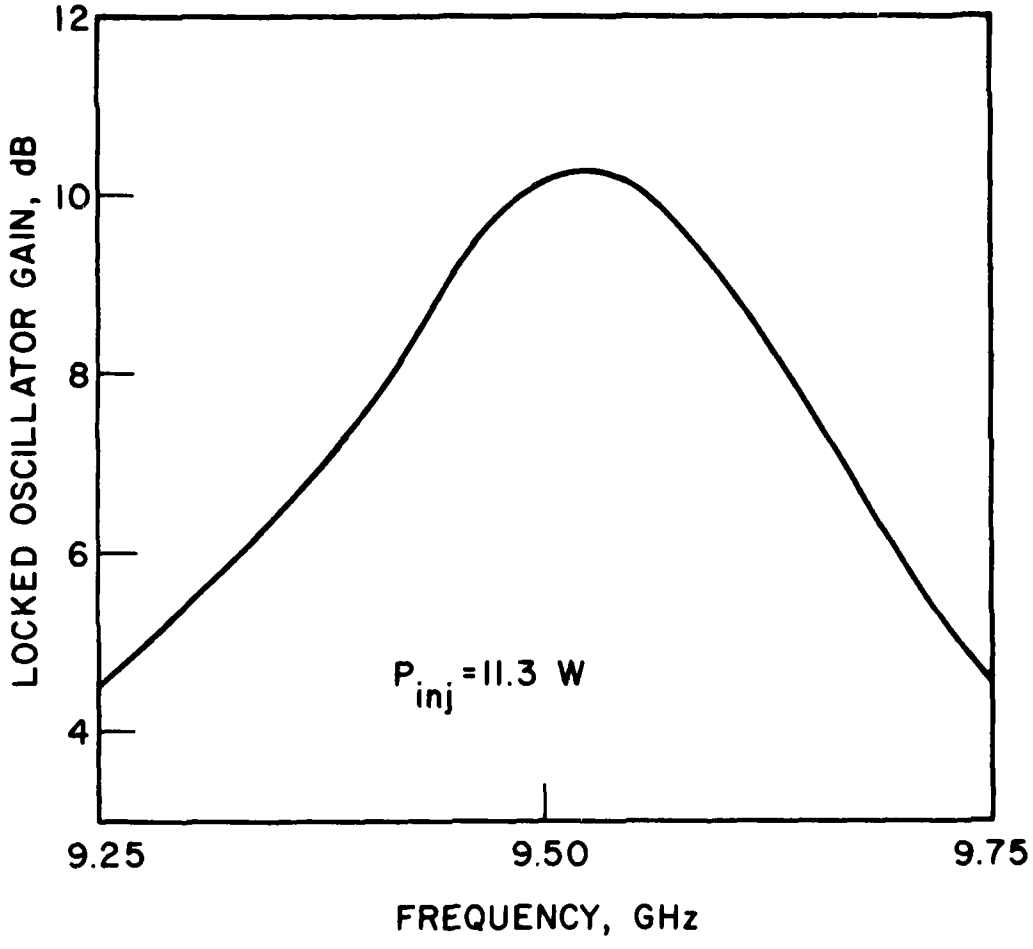


FIG. 26 LOCKED OSCILLATOR GAIN VS. FREQUENCY OBTAINED FROM THE CURVE OF FIG. 25. The 1-dB BANDWIDTH HAS REDUCED TO 150 MHz FOR THE FACTOR OF FOUR INCREASE IN POWER OUTPUT.

Again, the design of these combiners is not based on the conventional concepts of "match" and "isolation" useful in other power dividing/adding arrays of sources or amplifiers. The negative-resistance properties of the device bring about new and more appropriate constraints on line impedance levels, lengths and stabilization (isolation) resistances.

Certain additional aspects of these combiners including the existence of "other" modes of oscillation; effects of nonidentical devices; device failure on power output; and two-section, capacitively stabilized lossless combiners are analyzed in Appendices A through C.

It is concluded from this work that this approach to power combining provides as good and often better performance than other combining schemes.[1] At X-band, the lossless combiner demonstrated a locked oscillator bandwidth several times larger than the TM_{ono}-mode combiners in a simpler geometry. The results at millimeter wavelengths indicate that this approach could yield high power and substantial bandwidths but integrated circuit techniques would be required for combiner realization. Use of "fork" style combiners rather than radial-symmetric types are likely candidates for combiner integrated circuit realizations at millimeter wavelengths.

Appendix A. Other Modes of Oscillation

The fact that the active devices in a power combiner are nonlinear and probably nonidentical allows other modes of oscillation to exist than those indicated in Section 2. This was pointed out by Kurokawa[9] in his analysis of Rucker's circuit.[8] In this Appendix, some design guidelines are developed for dealing with other modes of oscillation and the effects of nonidentical devices.

In the case of degenerate eigenvalue combiners, specific design criteria can be developed through simple geometric interpretations. For nondegenerate networks, design criteria are more difficult to establish.

Oscillation Condition. The oscillation condition (Eq. 8) can be written as

$$(\underline{Y} + \underline{Y}_t')\underline{V}' = \underline{A} = \left(\frac{y_{od}^2}{y_{oo} + Y_L} \sum_{k=1}^{N} V_k\right)\sqrt{5}\underline{X}_o \tag{50}$$

which can be examined for any value of $\underline{A}$ to determine modes other than the zeroth and rotating ones established in Section 2. Analysis and determination of these other modes will be attempted systematically by first considering the degenerate eigenvalue case for identical and nonidentical devices and then investigating the nondegenerate circuit situation.

Degenerate Networks--Identical Devices. For a power combining network $\underline{Y}$ which has $y_{ij} = 0$ for $i \neq j$ or equivalently

$$\underline{Y} = y_{11}\underline{I} \quad , \tag{51}$$

the eigenvalues λ_n are given by

$$\lambda_o = y_{11} - \frac{Ny_{od}^2}{y_{oo} + Y_L} \tag{52a}$$

and

$$\lambda_n = y_{11} \quad , \quad n = 1,2,\ldots,N-1 \quad . \tag{52b}$$

Hence the λ_n, $n > 1$ are degenerate. In addition, if identical devices

are assumed, i.e.,

$$Y_{dk}(V) = Y_d(V) \tag{53}$$

so they all have the same admittance function, then Eq. 50 can be written as

$$[y_{11} + Y_d(|V_k|)]V_k = A \quad , \quad k = 1,2,\ldots,N \quad . \tag{54}$$

The cophase (even) and antiphase (rotating) modes are found from Eq. 54 as in Section 2, i.e., $\lambda_n + Y_d(|V_K|) = 0$, $n = 0,1,\ldots,N-1$. Of interest here is whether a mode other than the zeroth can exist for finite A.

Kurokawa[9] examined Eq. 54 in a perturbation analysis for $\lambda_1 >> \lambda_o$ (except on an impedance basis) and found the zeroth mode can be perturbed only if

$$\lambda_1 - \lambda_o = \frac{N y_{od}^2}{y_{oo} + Y_L} = - V_o \left.\frac{\partial Y_d}{\partial V_o}\right|_{V_o} \quad , \tag{55a}$$

where

$$- Y_d(V_o) = \lambda_o \quad . \tag{55b}$$

As pointed out, Eq. 55a requires a highly unusual circumstance between device properties and circuit properties which are virtually independent of each other.

A stronger, more general condition than Eq. 55 can be derived which guarantees that only the zeroth mode can exist in the combiner. From Eq. 54 it is apparent that the only way the V_k's can differ from each other is if the solution for $|V_k|$ from Eq. 54 as a

function of $|A|$ is not single valued. Possible solutions for $|V_k|(|A|)$ from

$$\left|y_{11} + Y_d(|V_k|)\right||V_k| = |A| \tag{56}$$

for different values of y_{11} are shown in Fig. 27. Considering the cases indicated, the following arguments can be made:

1. If the function $|V_k|(|A|)$ is single valued, there is a unique solution V_k for $|A| > 0$ and hence all V_k's must be identical and have the zeroth mode value V determined by

$$[y_{11} + Y_d(V)]V = \frac{Ny_{od}^2}{y_{oo} + Y_L} \quad . \tag{57}$$

2. If the function is not single valued, then another mode <u>may</u> be possible <u>if</u> $|A|$ is in the hysteresis range (curve C in Fig. 27). Such a solution requires that

$$\sum_{k=1}^{N} V_k = \ell V_a + mV_b \quad , \quad \ell + m = N$$

with

$$|A|_{min} \leq \left|\frac{y_{od}^2 \sum_{k=1}^{N} V_k}{y_{oo} + Y_L}\right| \leq |A_{max}| \quad .$$

For a power combiner with a designed zeroth order mode (Y_L), such a solution would indeed require an unusual combination of device and circuit behavior.

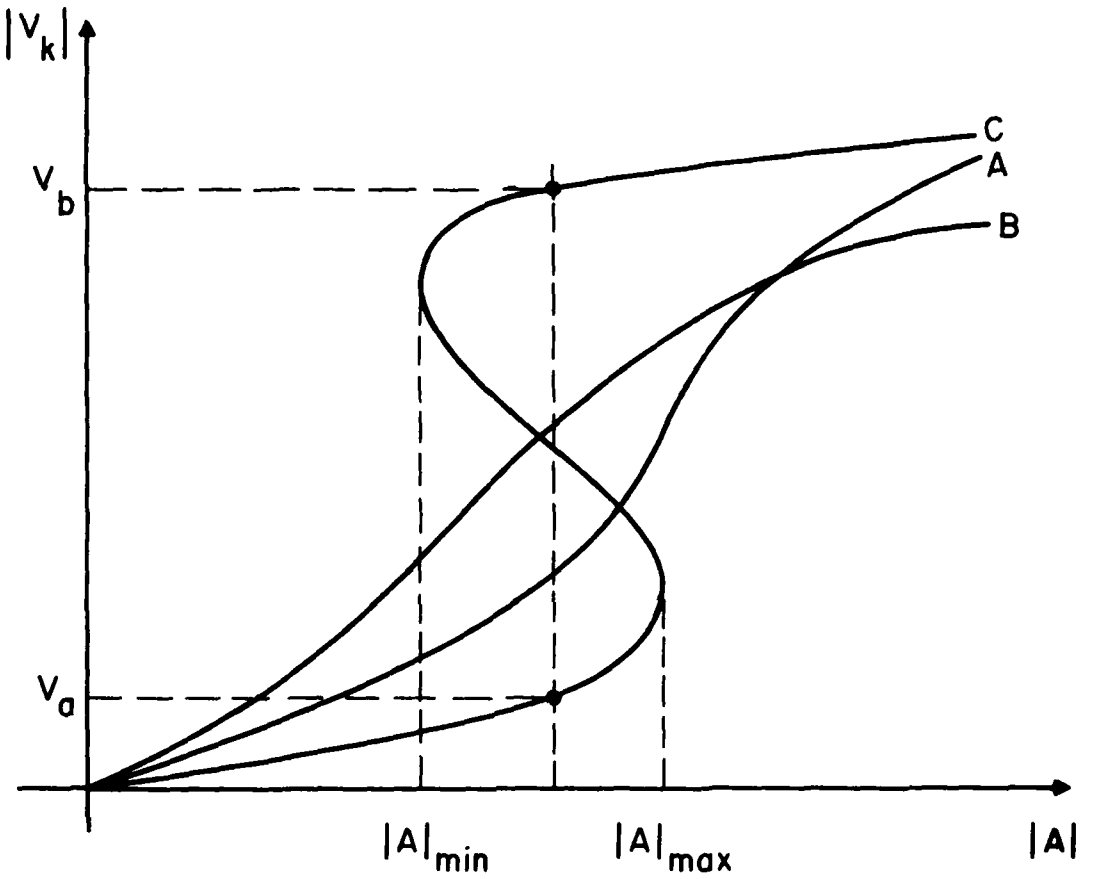


FIG. 27 VARIOUS SOLUTIONS TO THE EQUATION $|y_{11} + Y_d(V)||V| = A$ FOR DIFFERENT VALUES OF y_{11}. "OTHER" MODES ARE POSSIBLE BUT NOT PROBABLE FOR CASE "C."

While unlikely, the problem can be avoided by choosing y_{11} to ensure that the solution for $|V_k|$ in Eq. 56 is single valued for any frequency in the active bandwidth of the diode. The region of the complex plane to be avoided can be determined by setting $d|V_n|/d|A| \to \infty$ in Eq. 56, obtaining the result that

$$\left| y_{11} + Y_d(V) + \frac{V}{2} \frac{\partial Y_d}{\partial V} \right| \geq \frac{1}{2} V \left| \frac{\partial Y_d}{\partial V} \right| \qquad (58)$$

for stability. For a given value of V at any ω, the equality in Eq. 58 is the equation of a circle in the y_{11} plane. Considering all values of V at any ω results in a region as shown in Fig. 28 made up of a family of circles. Also indicated is Kurokawa's locus from Eq. 55. If y_{11} lies outside these circles, only the desired zeroth mode of oscillation can exist. The stability region must be determined for each frequency in the active bandwidth of the device. In the case of Rucker's circuit,[8] equivalently, y_{11} was large and positive real so that it did not generally lie in the instability region, unless the $Y_d(V)$ function had unusual properties.

It is apparent that if y_{11} avoids the region bounded by Eq. 58 for all active ω, then clearly $y_{11}(j\omega) + Y_d(j\omega,V) \neq 0$ and rotating mode stability is also guaranteed. Therefore for this identical-diode, degenerate-eigenvalue combiner, Eq. 58 allows only zeroth mode operation. Note that Eq. 58 is sufficient, but may not be necessary for stability of all undesired modes.

Degenerate Networks--Nonidentical Devices. For nonidentical devices, Eq. 54 is written as

$$[y_{11} + Y_{dk}(|V_k|)V_k = A \quad , \quad k = 1,2,\ldots,N \quad , \qquad (59)$$

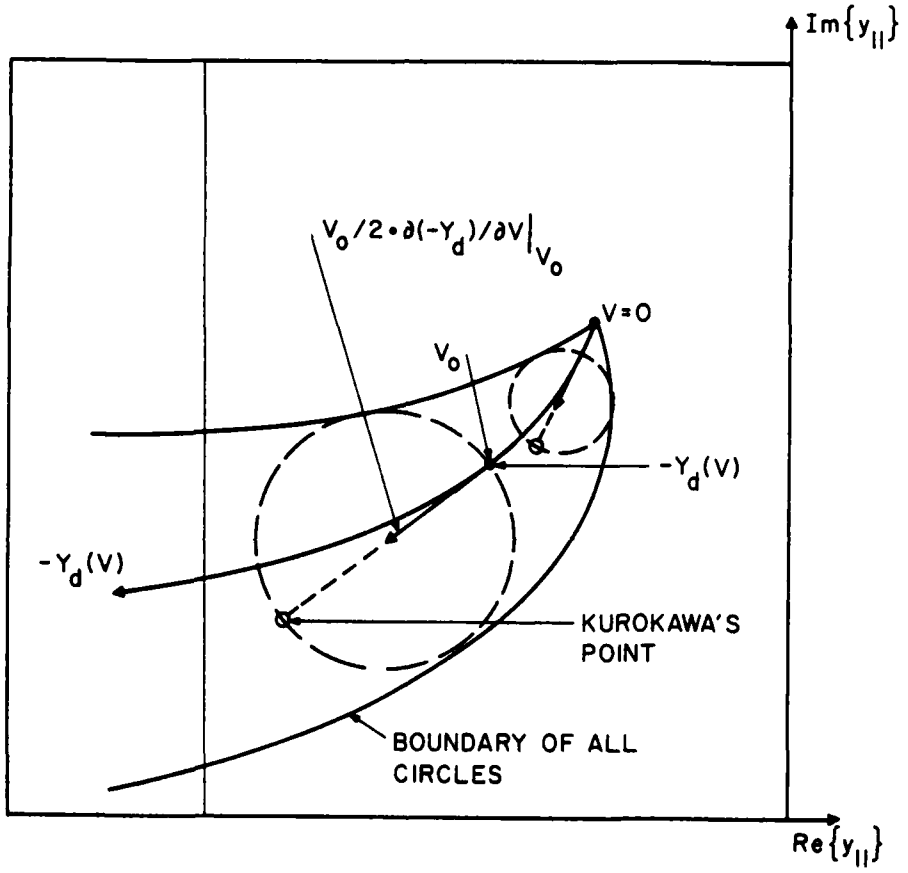


FIG. 28 THE REGION OF y_{11} ADMITTANCE WHICH PROVIDES HYSTERESIS IN THE V(A) CURVE (FIG. 27) AND THE POSSIBILITY OF OTHER MODES. KUROKAWA'S POINT IS ALSO INDICATED.

where it is assumed that the solution for $|V_k|(|A|)$ is a single-valued function. If the Y_{dk} functions are somewhat different from each other, then the V_k's from Eq. 59 will differ in amplitude and phase. The amount of phase and amplitude differences required can be visualized graphically by plotting the functions $[y_{11} + Y_{dk}(V)]V$, where V is an RF amplitude. A typical plot of one of these functions is constructed as shown in Fig. 29, and Fig. 30 indicates how several functions for different diodes may appear. Also shown in Fig. 30 is a circle corresponding to $|A|$ = constant. The intersection of this circle with any curve determines the associated value of $|V_k|$, and the phase of V_k relative to that of A is determined by the angular rotation required for the intersection to reach some chosen point A on the circle. The phase of A is not important, only the relative phase shifts required among the various curves. Hence the maximum phase difference of all the diode voltages is δ as shown.

From a design standpoint, the optimum situation might be to use the value of $|A|$ for maximum total output power. If the functions $Y_{dk}(V)$ are known, then the value of $|A|$ would be chosen such that the solutions for $|V_k|(|A|)$ from

$$|y_{11} + Y_{dk}(|V_k|)|\,|V_k| = |A| \quad , \quad k = 1,2,\ldots,N \tag{60}$$

would maximize the total generated power P_{gT} given by

$$P_{gT}(|A|) = \frac{1}{2}\sum_{k=1}^{N} \mathrm{Re}\{Y_{dk}[|V_k|(|A|)]\}|V_k|^2(|A|) \quad . \tag{61}$$

From the value of $|A|$, the relative phases of the V_k can be found, so that the proper load admittance Y_L for the oscillator can be found

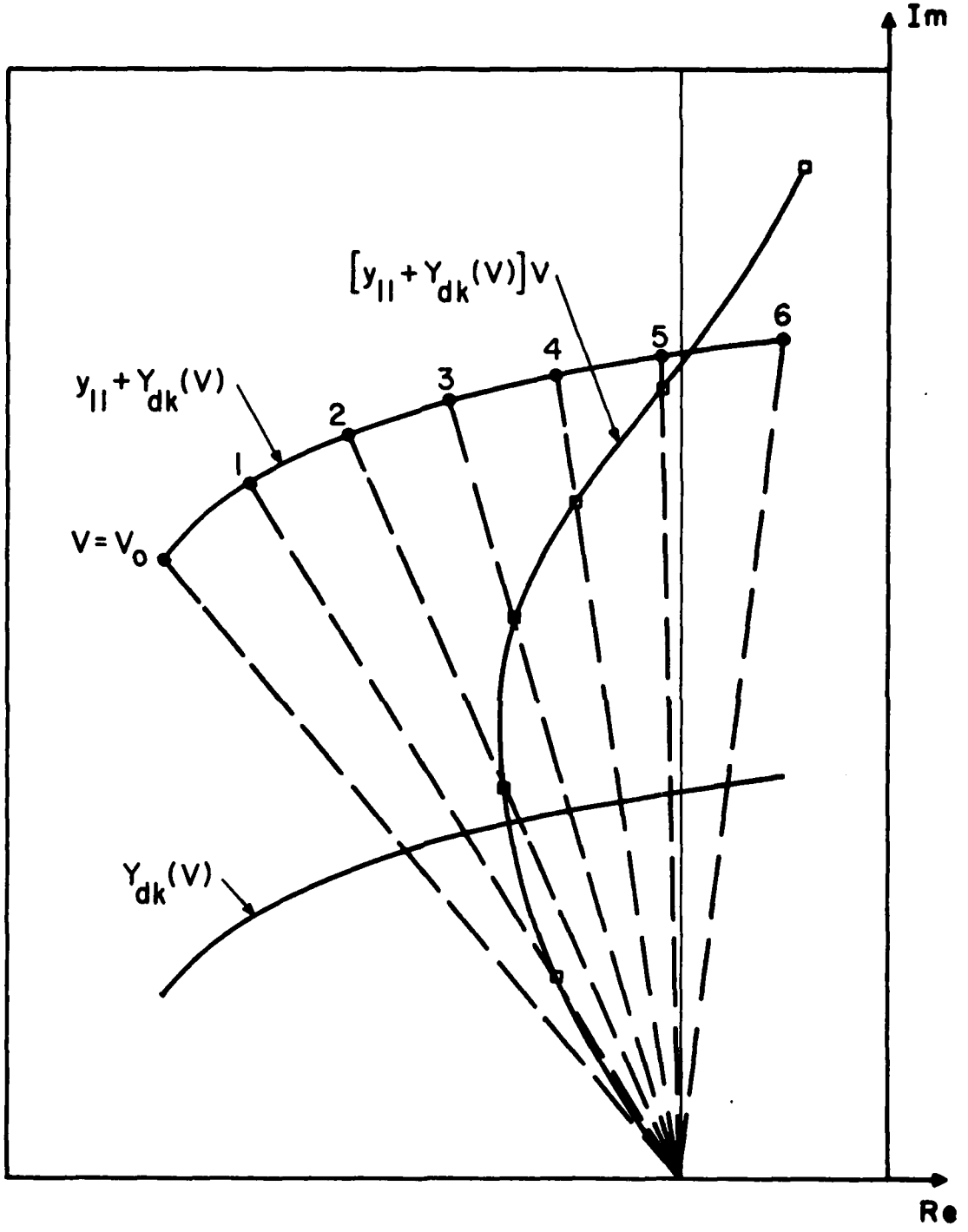


FIG. 29 DETERMINATION OF THE FUNCTION $[y_{11} + Y_d(V)]V$ FOR A GIVEN DIODE FOR USE IN COMPARING WITH OTHER DIODES.

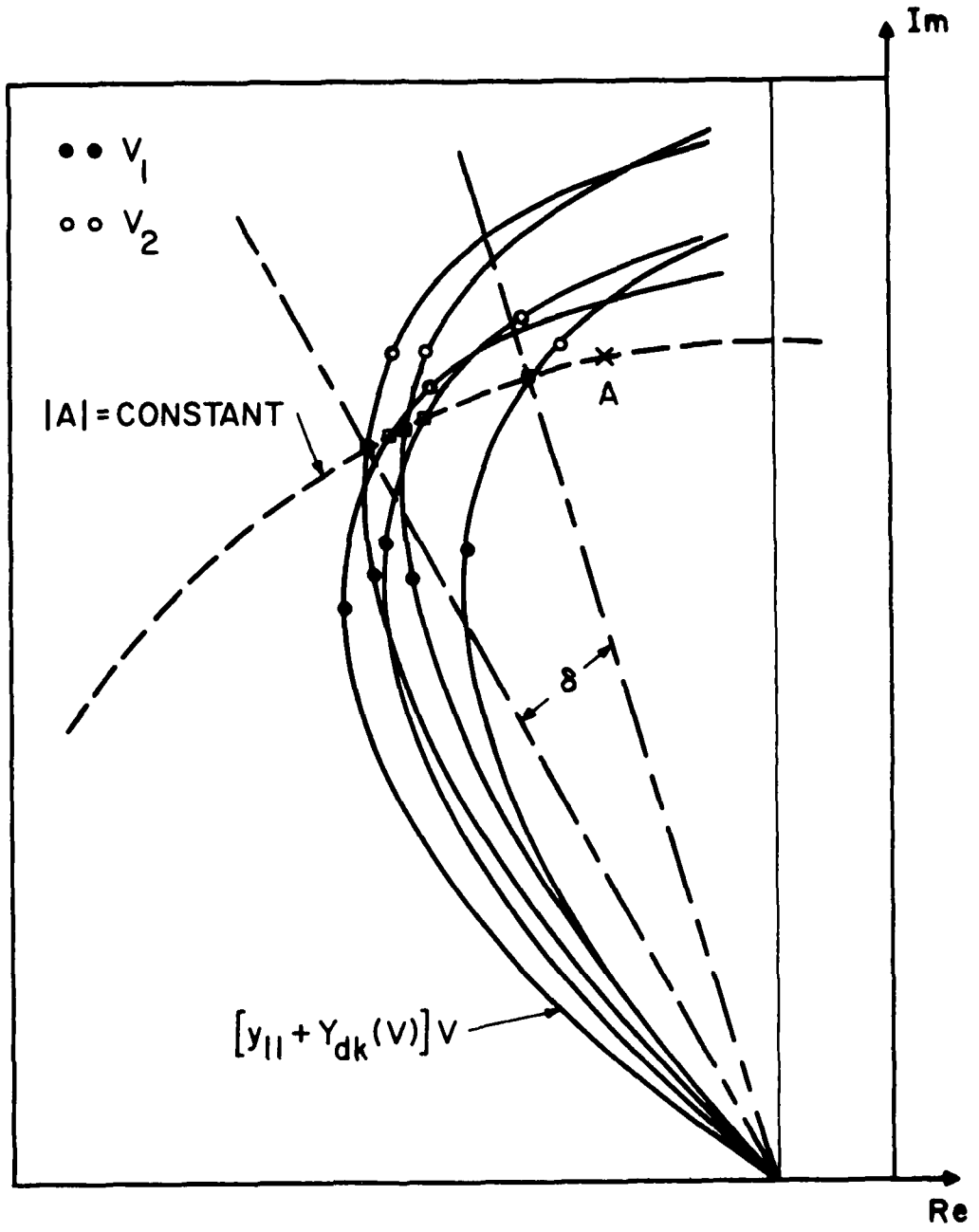


FIG. 30 GRAPHICAL EXPLANATION OF THE AMPLITUDE AND PHASE VARIATIONS OCCURRING WHEN NONIDENTICAL DIODES ARE COMBINED. THE MAXIMUM PHASE VARIATION AMONG THE DIODES IS δ. THE VALUE OF A CAN BE ADJUSTED TO MAXIMIZE THE TOTAL POWER.

from

$$[y_{11} + Y_{dk}(|V_k|)]V_k = \frac{y_{od}^2}{y_{oo} + Y_L} \sum_{n=1}^{N} V_n \quad , \tag{62}$$

which is satisfied for any k value.

If the Y_{dk} deviate only slightly from one another, a perturbation analysis of Eq. 59 can be used to predict expected output levels if the deviation statistics of the device admittance is specified. Optimal solutions to Eqs. 60 through 62 give the desired mode of operation and represent a "perturbed" zeroth mode compared to the case of identical devices. Since the solution to Eq. 59 was assumed single valued, Eq. 58 holds for each $Y_{dk}(V)$ function and hence this perturbed zeroth mode is the only one possible.

General Case--Nondegenerate Eigenvalues and Nonidentical Devices. In the more general case when the λ_n are not degenerate, stability for other modes does not have as straightforward an interpretation between device and circuit interaction. The condition that V_n be single valued for any value of A or any set $\{V_n\}$ is a sufficient criterion, but again may not be necessary. From Eq. 50

$$\underline{V}' = [\underline{Y} + \underline{Y}_t']^{-1}\underline{A} \triangleq \underline{MA} \tag{63}$$

so that

$$V_n = A \sum_{j=1}^{N} m_{nj} \tag{64}$$

and

$$|V_n| = |A|M_n \quad , \tag{65}$$

where $M_n = \left| \sum_{j=1}^{N} m_{nj} \right| = M_n(|V_1|, |V_2|, \ldots, |V_N|)$. Then,

$$d|V_n| = M_n d|A| + |A| \sum_{j=1}^{N} \frac{\partial M_n}{\partial |V_j|} d|V_j| \tag{66}$$

which gives

$$[\underline{I} - |A|\underline{P}] \frac{d|\underline{V}'|}{d|A|} = \underline{Q} \quad , \tag{67}$$

where $\underline{P} = [p_{ij}]$ with

$$p_{ij} = \frac{\partial M_i}{\partial |V_j|} \tag{68}$$

and

$$\underline{Q} = [M_1, M_2, \ldots, M_N]^+ \quad . \tag{69}$$

It is clear from Eq. 67 that if the real matrix $\underline{I} - A\underline{P}$ is ever singular for any combination of $|V_n|$'s, some $|V_n|$ can have more than one value for a given $|A|$. In the case when all $|V_n|$ are small and Y_{dn} approaches its small-signal value and becomes essentially linear, normally $\underline{P} \to \underline{0}$ and $\underline{I} - A\underline{P}$ is a positive definite matrix. Hence, if $\underline{I} - A\underline{P}$ is always positive definite, finite output from the combiner will only occur in the zeroth or perturbed zeroth mode. For the degenerate case, Eq. 67 reduces to Eq. 58 as expected. In general, however, such lucid geometric interpretations as in Figs. 28 through 30 are not apparent.

With regard to these "other modes," a final comment is in order. It was shown for the degenerate case that even if Eq. 58 is not satisfied, a very unusual circumstance is required to have an instability

other than the zeroth mode, particularly when the circuit has been designed for the zeroth mode. It is suspected that the same is true for the nondegenerate case, that if designed for zeroth-order mode and for rotating mode suppression, the combiner will be very unlikely to oscillate in any other mode.

Appendix B. Diode Failure in Lossless, Degenerate Eigenvalue Networks

An N-diode TEM-line combiner as in Fig. 2 can be modeled as shown in Fig. 31a. If identical diodes are assumed, each generating a power P_g in the even mode, then clearly the total generated power P_{gN} is

$$P_{gN} = NP_g \quad . \tag{70}$$

If a single diode should fail such that it becomes passive, it reflects a passive impedance across the combining point and leaves N - 1 diodes active. The equivalent circuit for this situation is then as indicated in Fig. 31b, where $Y_{df}(\omega)$ is the passive admittance of the failed diode and Y_f is the admittance resulting from the transformation of Y_{df} through the TEM line. It is clear from Fig. 31b that certain values of Y_{df} and resulting Y_f can be disastrous, especially if Y_f becomes large approaching a short circuit. As with all failure analysis, results can only be obtained if Y_{df} is specified.

In the case of a single failure, the new load admittance Y_{Lf} is

$$Y_{Lf} = Y_L + Y_f \tag{71}$$

which is shared equally among N - 1 diodes. If $Y_{dt}(\omega,V)$ is the admittance of the diode transformed through the line to the

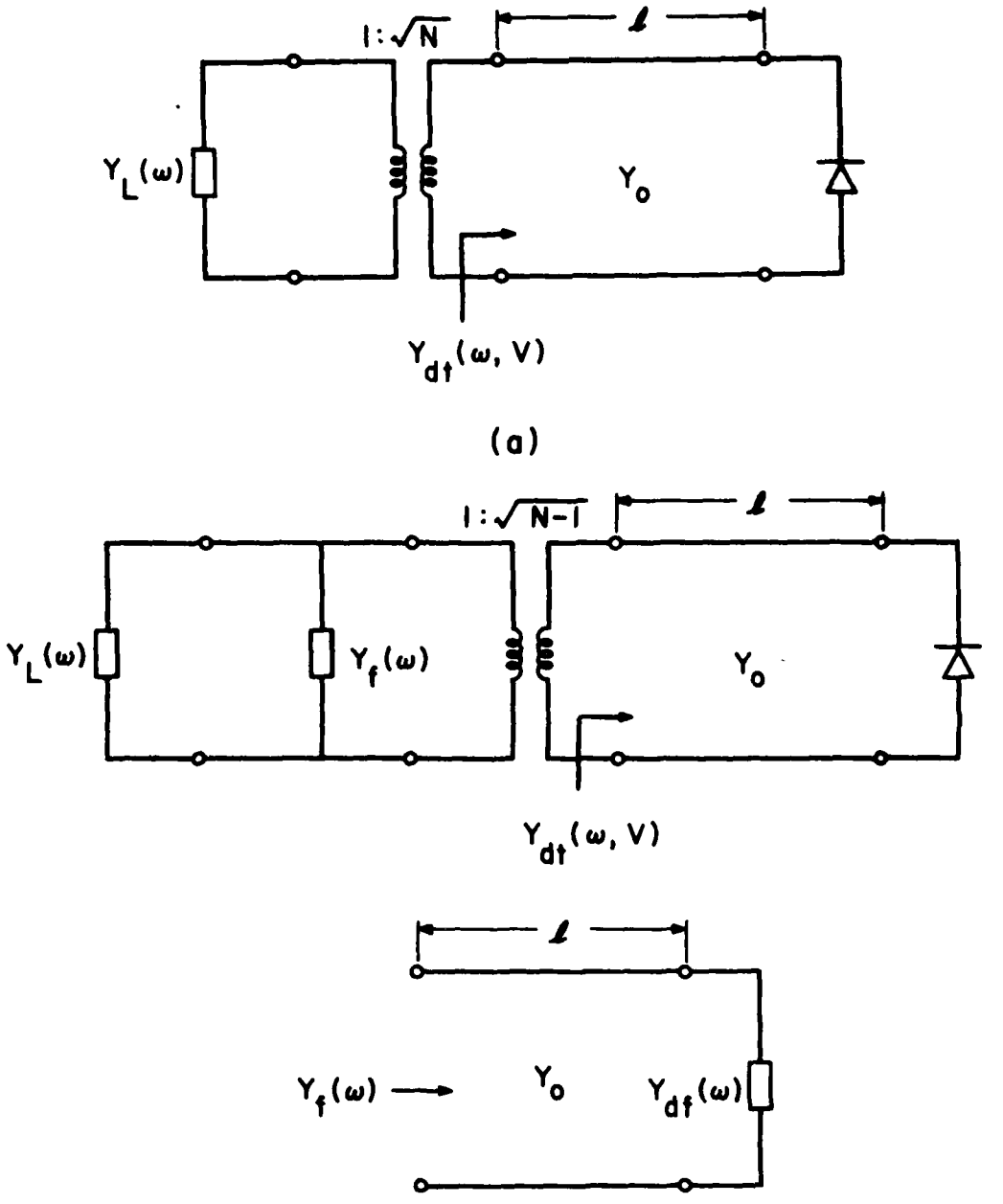


FIG. 31 (a) CIRCUIT MODEL FOR N-DIODE, LOSSLESS TEM-LINE COMBINER.

(b) CIRCUIT MODEL FOR COMBINER IN THE CASE OF A SINGLE DIODE FAILURE WHERE Y_{df} IS THE DIODE FAILED ADMITTANCE AND Y_f IS ITS TRANSFORMED VALUE AT THE COMBINING POINT.

combining point, the oscillation conditions for the cases of N diodes and N - 1 diodes are then

$$Y_{dt}(\omega_o,V_o) + \frac{Y_L(\omega_o)}{N} = 0 \quad (N \text{ diodes}) \tag{72a}$$

and

$$Y_{dt}(\omega_1,V_1) + \frac{Y_L(\omega_1) + Y_f(\omega_1)}{N-1} = 0 \quad (N-1 \text{ diodes}) \quad , \tag{72b}$$

where V_o and V_1 are the RF voltage amplitudes and ω_o and ω_1 are the oscillation frequencies for the N diodes and N - 1 diodes, respectively. Equation 72b can be written as

$$Y_{dt}(\omega_1,V_1) + \left(\frac{N}{N-1}\right)\frac{Y_L(\omega_1)}{N} + \frac{Y_f(\omega_1)}{N-1} = 0 \quad , \tag{73}$$

showing that the effect of the failed diode is shared equally among the remaining N - 1 devices. Thus for N reasonably large it is reasonable to expect that the effect of Y_f will result in only a small perturbation of ω and V from the values ω_o and V_o.

As seen in the examples of Section 3, the behavior of Y_{dt} around the design frequency can be modeled by a nearly frequency independent real part $G_{dt}(V)$. In addition, Y_{dt} is assumed resonant at ω_o so that $Y_L(\omega) = G_L$, a constant conductance. Furthermore, if the diode fails as a short or an open, Y_f may be considered lossless with respect to Y_L and Eq. 73 becomes

$$Y_{dt}(\omega,V) + \left(\frac{N}{N-1}\right)\frac{G_L}{N} + \frac{jB_f(\omega)}{N-1} = 0 \quad . \tag{74}$$

Hence, using Eq. 72a with Eq. 74 requires that

$$G_{dt}(V_1) = \frac{N}{N-1} G_{dt}(V_o) \tag{75a}$$

and

$$B_{dt}(\omega_1, V_1) = -\frac{B_f(\omega_1)}{N-1} \quad . \tag{75b}$$

The new operating voltage V_1 can be found from Eq. 75b and is used to find the new generated power. The frequency change is available from Eq. 75b.

For reasonable values of N, the change in V from Eq. 75a is expected to be small so that $G_{dt}(V)$ is approximated by

$$G_{dt}(V) = G_{dt}(V_o) + gv \quad , \tag{76}$$

where $v = V - V_o$. If V_o is selected for the maximum power generated, then

$$P_g(V) \cong P_{go}(V_o) + \left.\frac{\partial^2 P_g}{\partial V^2}\right|_{V_o} \frac{v^2}{2} \quad , \tag{77}$$

where it has been assumed that $(\partial P_g/\partial V)\big|_{V_o} = 0$. Using Eqs. 75a and 76 gives

$$v = \frac{G_{do}}{g}\left(\frac{1}{N-1}\right) \quad , \tag{78}$$

where $G_{do} = G_{dt}(V_o)$. Since

$$P_g = -\frac{1}{2} G_{dt}(V) V^2 \quad , \tag{79}$$

Eq. 77 becomes

$$P_g = -\frac{1}{2} G_{do} V_o^2 \left(1 - \frac{3}{4} \frac{1}{(N-1)^2}\right) \quad , \tag{80}$$

where $2V_o = -2G_{do}$ has been used from the fact that $(\partial P_g/\partial V)\big|_{V_o} = 0$. Now the total output power from the N - 1 devices P_{gN-1} relative to that for the N devices is simply

$$\frac{P_{g,N-1}}{P_{gN}} = \frac{N-1}{N}\left(1 - \frac{3}{4}\,\frac{1}{(N-1)^2}\right) \tag{81}$$

which, for large N, goes as (N - 1)/N and is "graceful." It is interesting that initial operation at the maximum point on the device curves results in such a simple power degradation.

The frequency shift of the free-running oscillator can be obtained from Eq. 75b if $B_f(\omega)$ is known. If the oscillator was initially injection locked, then it may or may not remain locked depending on the size of $B_f(\omega)$. If $B_f \neq 0$, the injected power will need to be increased to obtain the added power level of Eq. 80.

It is concluded that the effect on performance of a diode failure for the lossless degenerate eigenvalue combiner is no worse than with other combiners[1] and may be even better in many cases. For large N, Eq. 81 can be extended to M devices if M << N so that Eq. 76 remains valid. The result of Eq. 81 is close to the degradation recently predicted by Saleh[14] for a lossless output "matched" combiner of N amplifiers. In his analyses, where each amplifier output was modeled as a linear source, it was shown that a degradation given by

$$\frac{P_{o,N-M}}{P_{o,N}} = \left(1 - \frac{M}{2N - M}\right)^2 \tag{82}$$

could be obtained where M is the number of failed amplifiers. Assuming Eq. 76 is valid gives Eq. 81 for M failed amplifiers as

$$\frac{P_{g,N-M}}{P_{g,N}} = \frac{N - M}{N}\left[1 - \frac{3}{4}\left(\frac{M}{N - M}\right)^2\right] \quad . \tag{83}$$

Plots of Eqs. 82 and 83 as functions of M/N are shown in Fig. 32 for $M/N \leq 0.5$. Both curves have the same slope of - 1 for small M/N. Of course, Eq. 83 may only be valid for small M/N, but it does account somewhat for device nonlinearities.

Appendix C. Use of Shunt Capacitance and Two-Section TEM Lines for Improved Stabilization

In combination with a single-section TEM line in a degenerate eigenvalue combiner, the diode properties specified by $B_{dg}(\omega)$ (see Section 3) results in constraints on line impedance level Z_o or the diode area, line impedance (AZ_o) product necessary for rotating mode stability. The use of shunt capacitance across the diode and/or a multiple TEM-line section can improve these Z_o or AZ_o constraints, adding design flexibility and improving combiner output power level. Some aspects of these techniques are given in this Appendix.

The effect of adding shunt capacitance on stability and design is very apparent for a diode having $B_c < 0$, $B_m > 0$. Limitations on $\overline{B}_m$ from Fig. 7 can be eliminated by adding enough shunt capacitance to make $B_c \geq 0$, thereby providing the desired stability while adding design flexibility in line impedance level or AZ_o product. Of course, the effective diode Q increases and the bandwidth capability reduces accordingly. However, in some cases this degradation may be tolerable, particularly if the alternative is impractical Z_o level or low output power.

In addition to shunt capacitance, two or more sections of TEM lines with appropriate impedance levels and line lengths can improve the stability margin and allow larger Z_o or AZ_o values in design.

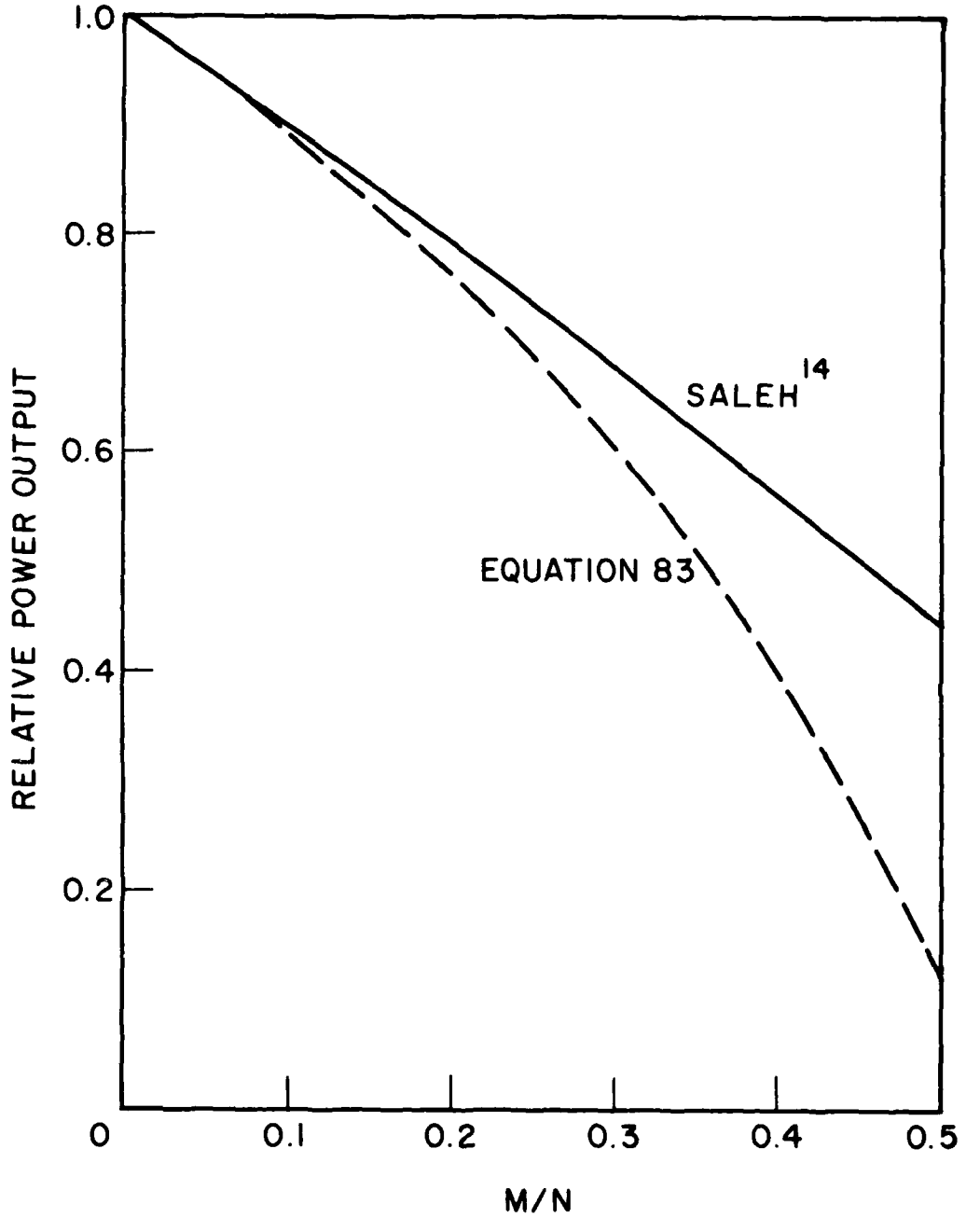


FIG. 32 A COMPARISON OF SALEH'S GRACEFUL DEGRADATION ASSOCIATED WITH IDEAL LINEAR AMPLIFIERS AND THAT OF EQ. 83 AS A FUNCTION OF THE RELATIVE NUMBER OF FAILED DEVICES.

Only two sections will be considered here, along with the effect of shunt capacitance, such that the equivalent combiner circuit will be as shown in Fig. 33. For this situation, the stability requirements similar to Eqs. 24a and b are given by

$$2[\theta_o + \tan^{-1} (r \tan \theta_1)] \geq \pi + 2 \tan^{-1} (-\bar{B}'_c) \qquad (84a)$$

and

$$2[\alpha\theta_o + \tan^{-1} (r \tan \alpha\theta_1)] \leq 2\pi - 2 \tan^{-1} \left(-\frac{1}{\bar{B}'_m}\right) , \qquad (84b)$$

where dispersionless lines are assumed and

θ_o = the electrical length of the Y_o-line at ω_c,

θ_1 = the electrical length of the Y_1-line at ω_c,

$r = Z_1/Z_o = Y_o/Y$,

$\alpha = \omega_m/\omega_c$,

and the primed quantities $\bar{B}'_m$ and $\bar{B}'_c$ include the shunt capacitance and are <u>normalized to</u> Y_o. For any specified values of $\bar{B}'_c$, and $\bar{B}'_m$ and α, Eqs. 84 provide two relations in three variables r, θ_o, and θ_1, so that a range of solutions are usually possible. It is probably most desirable to use the solution with the ratio r being closest to unity. For this case, the solutions to Eq. 84 for the equality can be found by suitable manipulation to be

$$\theta_1 = \frac{\pi}{1 + \alpha} , \qquad (85a)$$

$$\theta_o = \frac{A + B + (\pi/2)}{1 + \alpha} \qquad (85b)$$

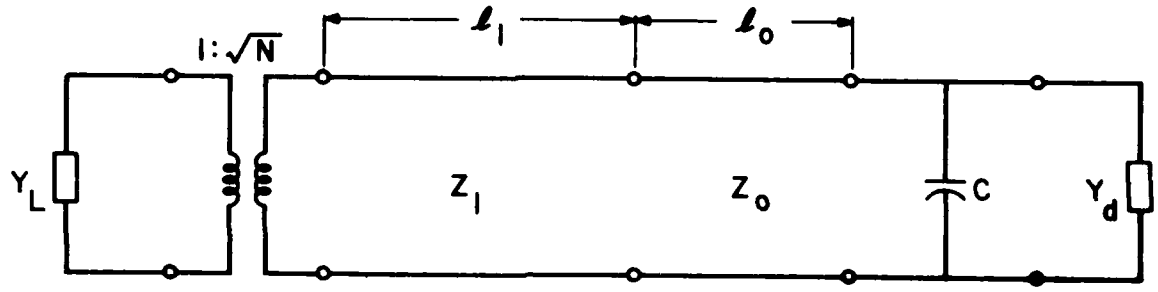


FIG. 33 A LOSSLESS, DEGENERATE EIGENVALUE COMBINER CIRCUIT MODEL CONSISTING OF TWO TEM-LINE SECTIONS AND A SHUNT CAPACITANCE USEFUL FOR IMPROVING STABILITY.

and

$$r = \frac{1}{\tan\theta \tan(\theta_o - B)} \quad , \tag{85c}$$

where

$$A = \tan^{-1}(1/\bar{B}_m') \tag{85d}$$

and

$$B = \tan^{-1}\bar{B}_c' = \tan^{-1}\rho\bar{B}_m' \tag{85e}$$

with $\rho = B_c/B_m$ as before. As compared to a single line section combiner, the maximum value of $\bar{B}_m$ can be increased by allowing a value for $r \neq 1$. Accordingly, higher Z_o or area-Z_o products can be realized and afford more design flexibility and increased output power per device.

As an example of this method, the millimeter-wave diode of Section 3 is considered. For a single section of TEM line in the combiner, the limitations on area impedance or power impedance were found to be

$$A_d Z_o = 1.33 \times 10^{-4} \text{ cm}^2\text{-}\Omega \tag{86a}$$

or

$$P_g Z_o = 9.68 \text{ W-}\Omega \quad , \tag{86b}$$

where A_d is the diode area and P_g is the maximum power generated by the device. Hence for high power from one of these devices, low Z_o values must be realized, which are difficult and impractical to achieve. Using the technique outlined above provides increased values of $A_d Z_o$ and $P_g Z_o$.

As a design goal, 1 W per diode in an impedance level of 35 to 40 Ω or more was desired, or $P_g Z_o \approx 40$ W-Ω. This is accomplished by adding the minimum amount of shunt capacitance in combination with a two-section line. Adding more shunt capacitance than the minimum required will provide a stability margin but will reduce bandwidth capability. The circuit parameters resulting from the solution to Eqs. 85 are then given by

$$A_d Z_o = 5.536 \times 10^{-4} \text{ cm}^2\text{-}\Omega \quad , \tag{87a}$$

$$P_g Z_o = 40.28 \text{ W-}\Omega \quad , \tag{87b}$$

$$\theta_o = 0.5041 \text{ rad at } 53 \text{ GHz}, \tag{87c}$$

$$\theta_1 = 0.9124 \text{ rad at } 53 \text{ GHz}, \tag{87d}$$

$$r = 1.402 \tag{87e}$$

and

$$C = 2.257 \times 10^{-9} \text{ f/cm}^2 \quad . \tag{87f}$$

Shown in Fig. 34 is the relation between b_{dg} for the diode and the negative eigenvalue susceptance associated with the rotating modes, or the circuit susceptance for a short circuit at the combining point. The circuit susceptance for a single-section line is also shown for reference.

With the two-section plus capacitance combining lines, the diode admittance at approximately 78 GHz rotates to the real axis at the combining point. Hence, for a locked oscillator gain of approximately 10 dB at 78 GHz, a load admittance $\overline{Y}_L/N$ of 0.10 normalized to Z_1 was chosen and assumed real over the frequency range of interest. The resulting circuit admittance seen by the diode for the even mode is

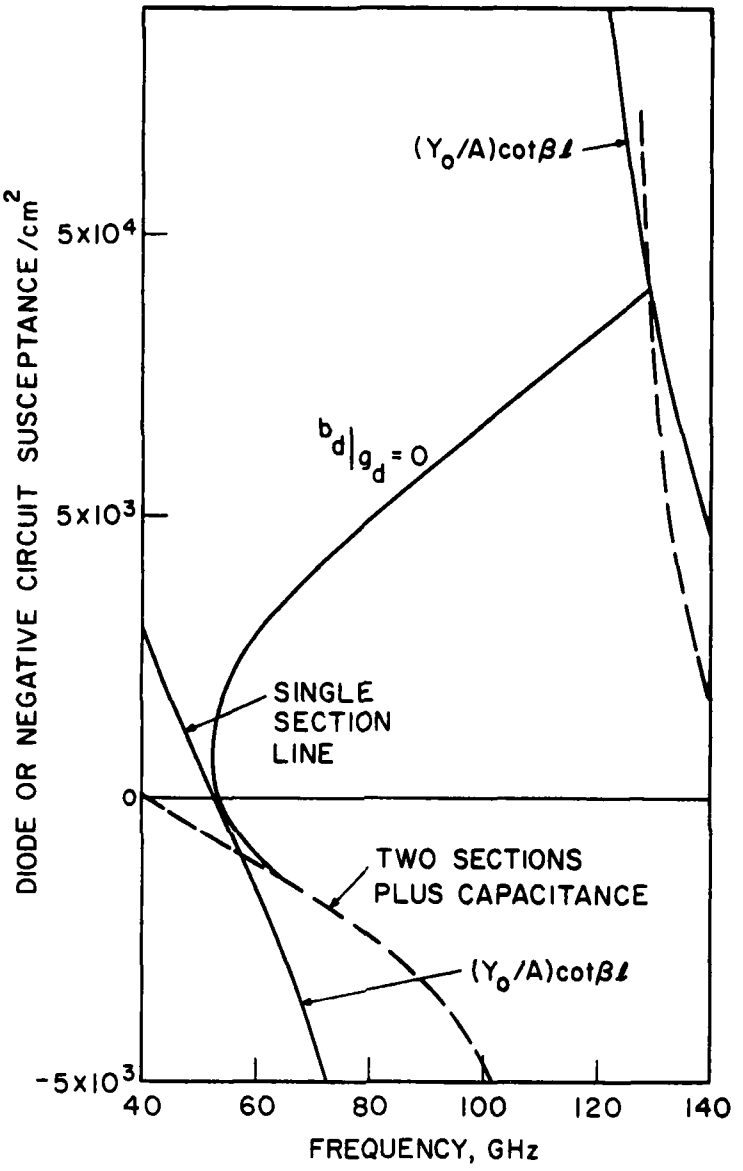


FIG. 34 DEVICE-CIRCUIT INTERACTION FOR THE MILLIMETER-WAVE DIODE EXAMPLE PERTINENT TO ROTATING MODE STABILITY. THE CIRCUIT ADMITTANCE FOR A TWO-SECTION LINE WITH CAPACITANCE RESULTING IN A FOURFOLD INCREASE IN POWER-IMPEDANCE PRODUCT IS SHOWN AND COMPARED TO THE SINGLE-SECTION CASE.

shown in Fig. 35, along with the trajectory of the locked oscillator around the center frequency. Lower bandwidth than that available with a single-section line (see Figs. 18 and 19) is indicated as expected. The locked oscillator gain vs. frequency is shown in Fig. 36 where the input power per diode is given as

$$\frac{P_{inj} Z_o}{N} = 4.41 \text{ W-}\Omega \tag{88a}$$

so that the output power at 78 GHz is approximately

$$\frac{P_{out} Z_o}{N} = 44.1 \text{ W-}\Omega \ , \tag{88b}$$

or 1 W per diode for a $Z_o = 44\ \Omega$ system at a gain of 10. A 1-dB bandwidth of approximately 6.5 GHz at 78 GHz is available, as compared to 9 GHz at 88 GHz for the single-section line, which is not much of a reduction for the resulting four-fold increase in the $P_g Z_o$ product.

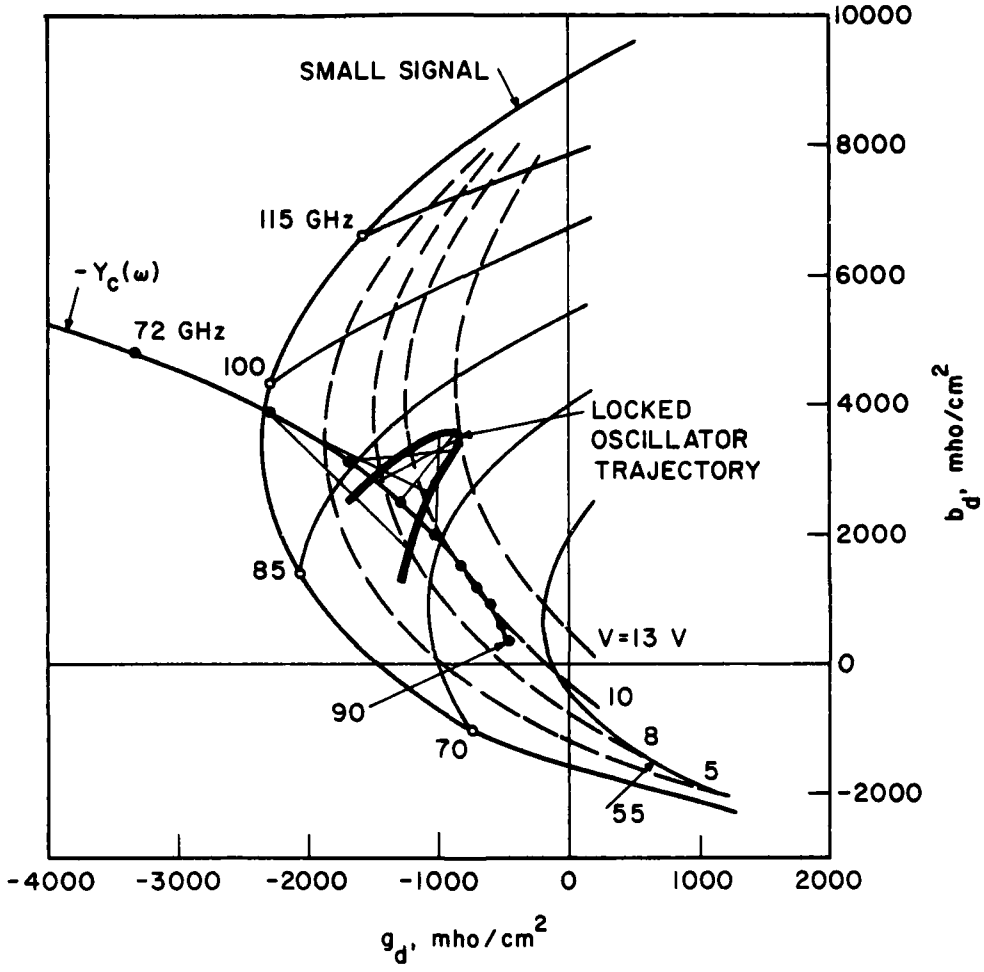


FIG. 35 LOCKED OSCILLATOR TRAJECTORY FOR THE TWO-SECTION LINE COMBINER DESIGNED FOR A CENTER FREQUENCY OF APPROXIMATELY 78 GHz. THE EVEN-MODE CIRCUIT ADMITTANCE IS ALSO SHOWN.

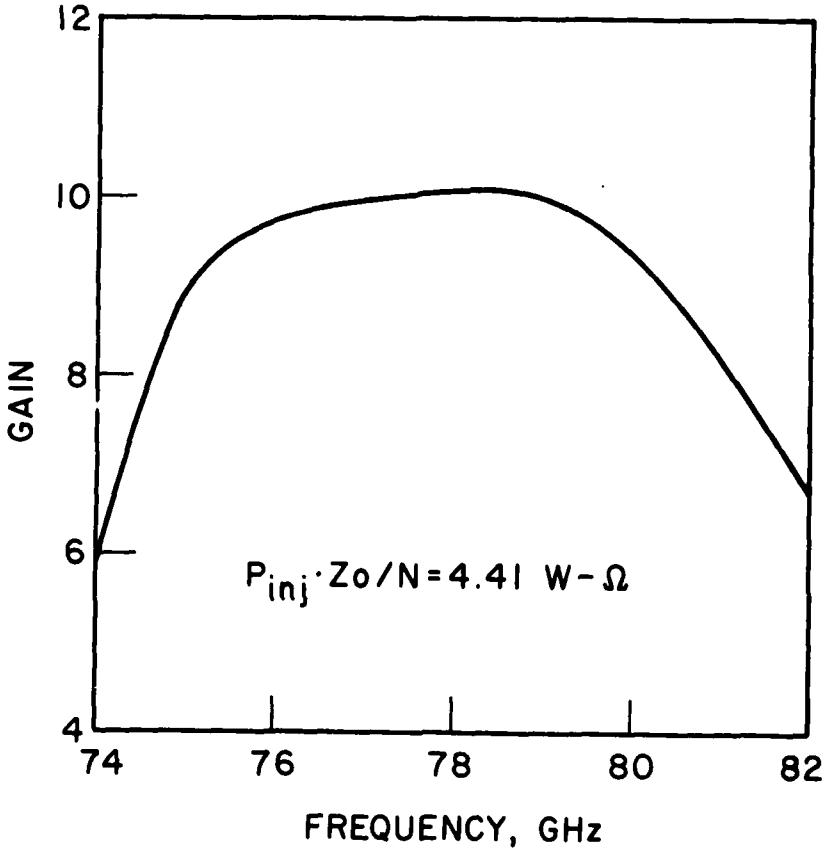


FIG. 36 LOCKED OSCILLATOR GAIN VS. FREQUENCY OBTAINED FROM FIG. 35. A 1-dB BANDWIDTH OF APPROXIMATELY 6.5 GHz IS OBSERVED. THIS RESULT CAN BE COMPARED TO FIG. 19. THE POWER-IMPEDANCE PRODUCT IS FOUR TIMES LARGER.